leti innovation for industry

Advanced top-down lithography challenges

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CEA - LETI
Silicon Technology Department

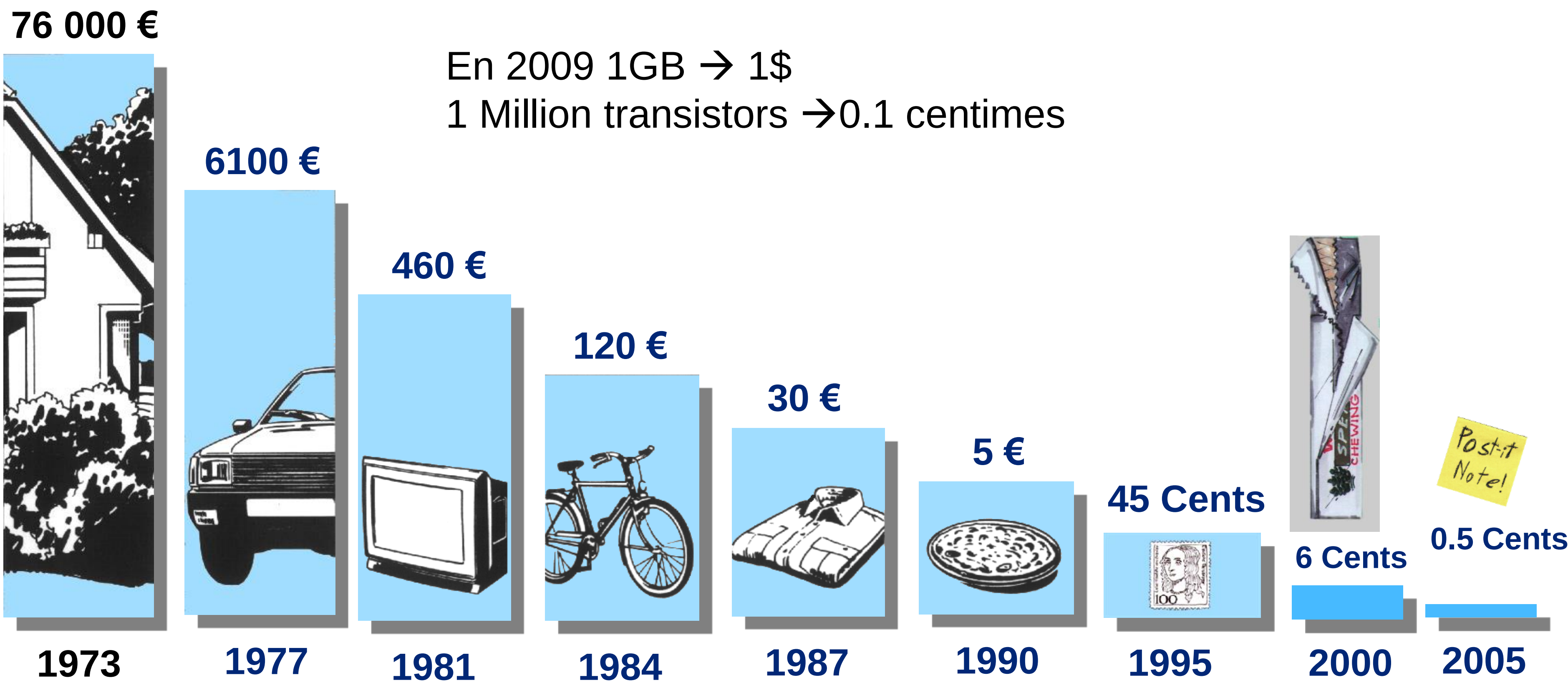
MINATEC CAMPUS

The microelectronics success story

A cost reduction unique in the industry history

PRIZE EVOLUTION OF 1 Million transistors

En 2009 1GB → 1$
1 Million transistors →0.1 centimes



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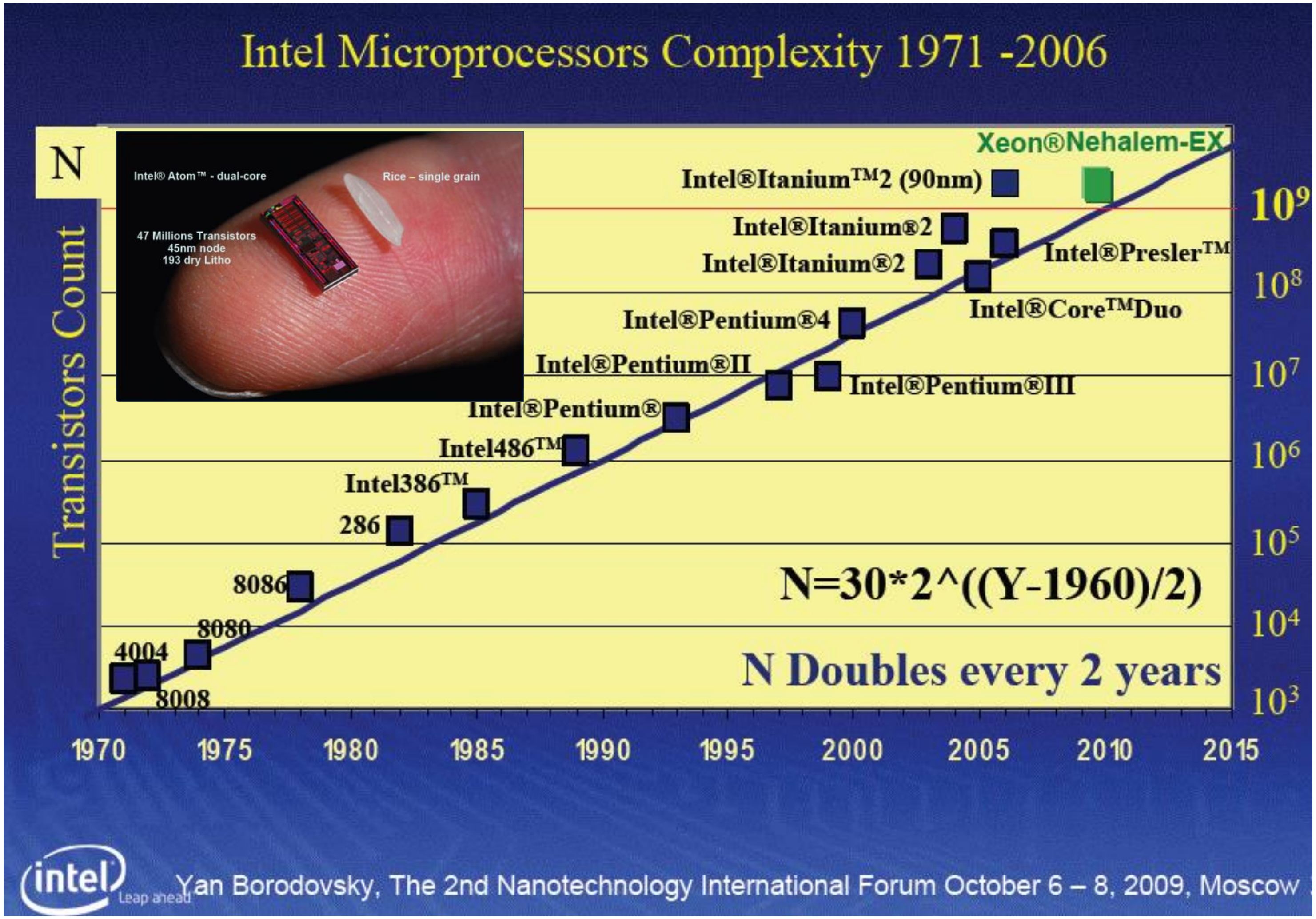
The Race to power…



<u>Moore's law</u>

Multiplication by 2 of transistor number in ICs every 18 months

At **<u>CONSTANT PRICE</u>**

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Why miniaturization ?
1st view

1971

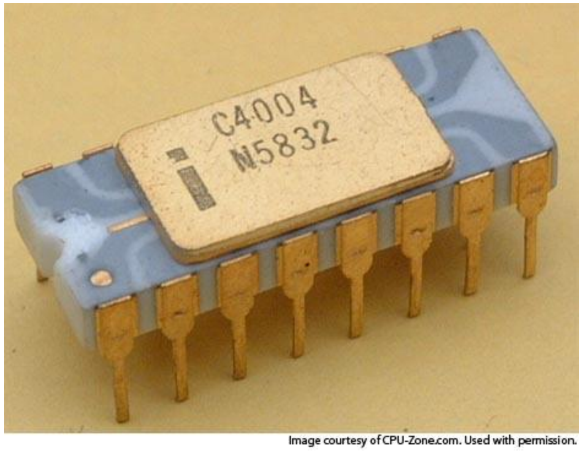
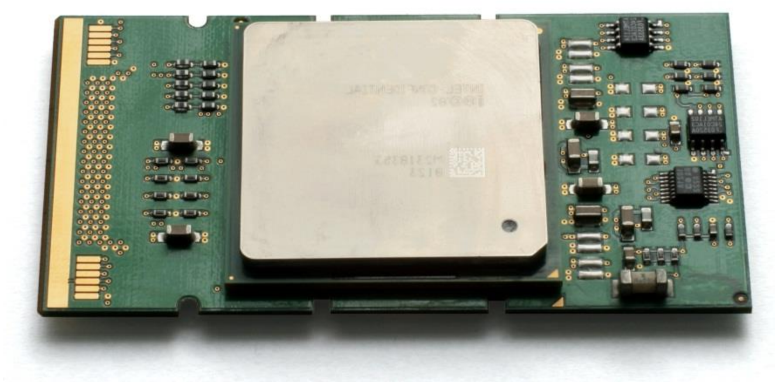


Image courtesy of CPU-Zone.com. Used with permission.

INTEL 4004
Surface : 90mm²
2,300 transistors

2005



INTEL ITANIUM 2
Surface : 698 mm²
1,000,000,000 transistors

X450,000

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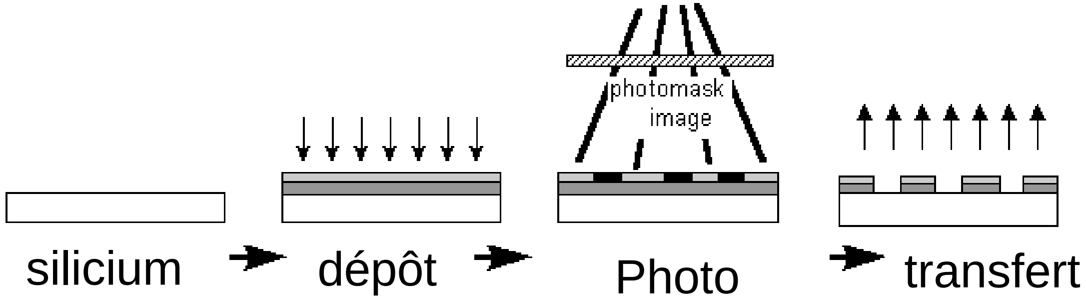
The lithography : The horse race of miniaturization

- Lithography : The way to realize IC circuits lines

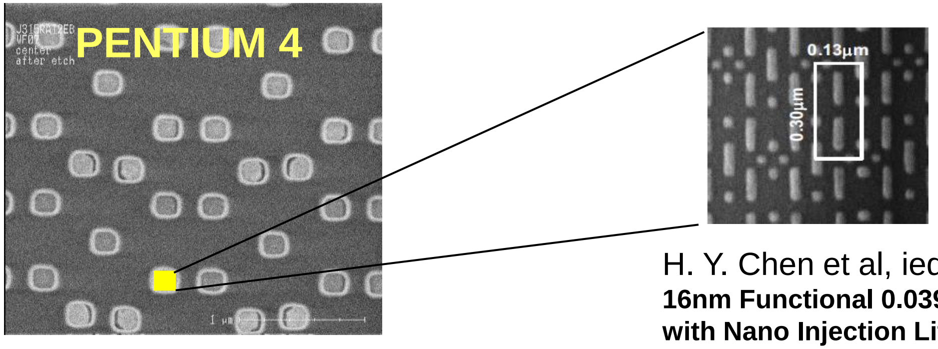


- Very simple challenges!
  - + and + smaller
  - + and + precize
  - - and - expensive

15 years

130nm node
2000

16nm node
2015



H. Y. Chen et al, iedm 2009
16nm Functional 0.039µm² 6T-SRAM Cell with Nano Injection Lithography, Nanowire Channel, and Full TiN Gate

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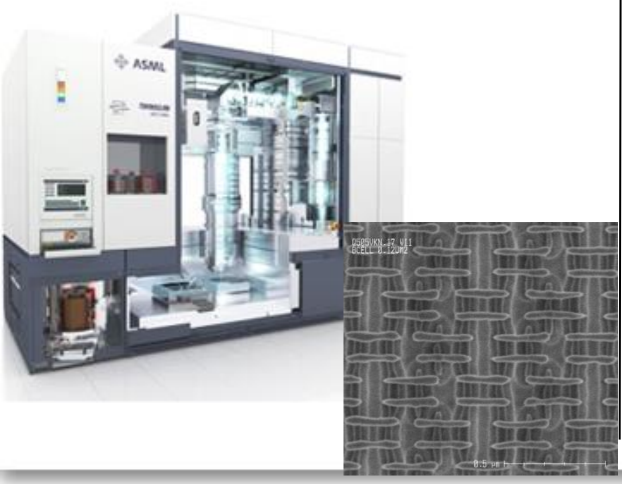
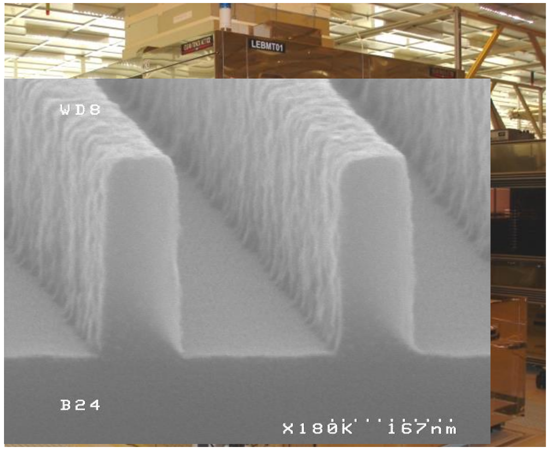
The toolbox of lithography?

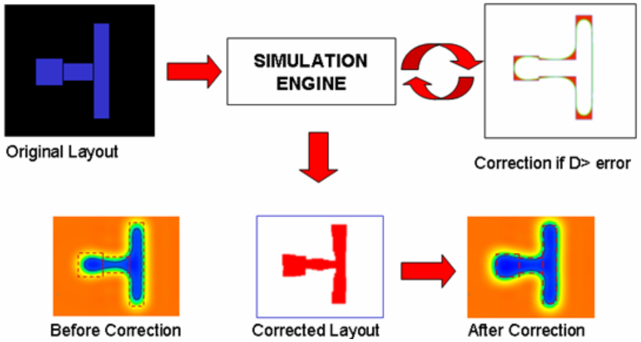
- Exposure tools
  - Exposition
    - Photons
    - Electrons
  - Resolution
    - Sub-20nm
  - Position accuracy
    - 2-5nm d'alignement
  - Throughput
    - >100wph

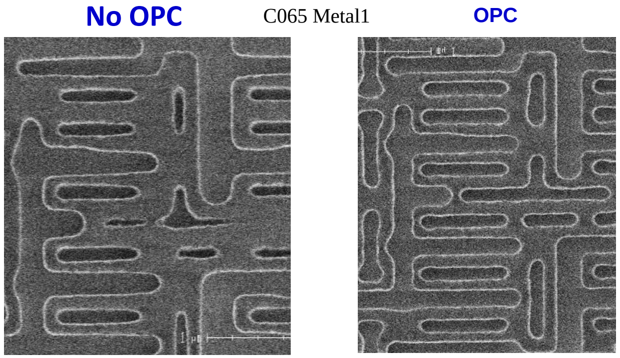


- Process
  - Resist
    - Photo sensitive
    - Resolution(<20nm)
    - Sensitivity (10mJ/cm²)
    - Transfer property
  - Process track
    - Fast (>200pl/h)
    - Repetable



- Proximity corrections
  - Corrections
  - Verification





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Lithography options for tomorrow

- Optical lithography
  - Resolution concern
  - Discussion on k1 improvement
  - Ultimate resolution for 193nm generation
  - EUV
- E-Beam direct write lithography
- Self Aligned Ligraphy by block copolymers
- Imprint lithograhy

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Optical lithography

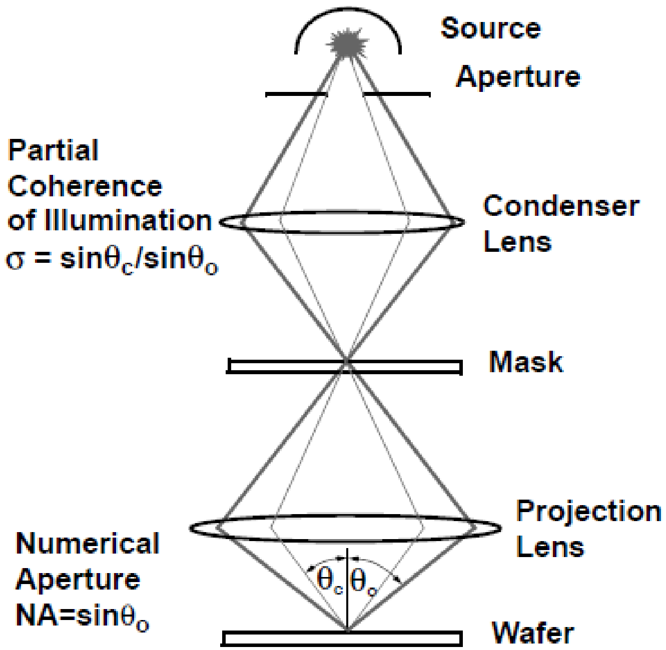
- Resolution driven by the Rayleigh criteria

$$R = k_1 \times \frac{\lambda}{NA}$$

$$DOF = k_2 \frac{\lambda}{NA^2}$$

$$with \quad NA = n \times \sin(\theta_0) < n$$

$$k_1 \; process\_factor$$



ASML/1950i

λ : 193nm
NA : 1.35
Resolution 38nm L/S
Overlay 3.5nm (3σ)
175 pwafers/h

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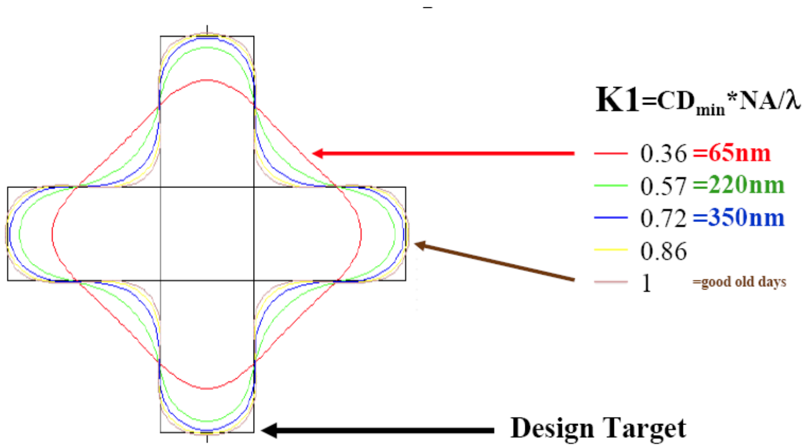
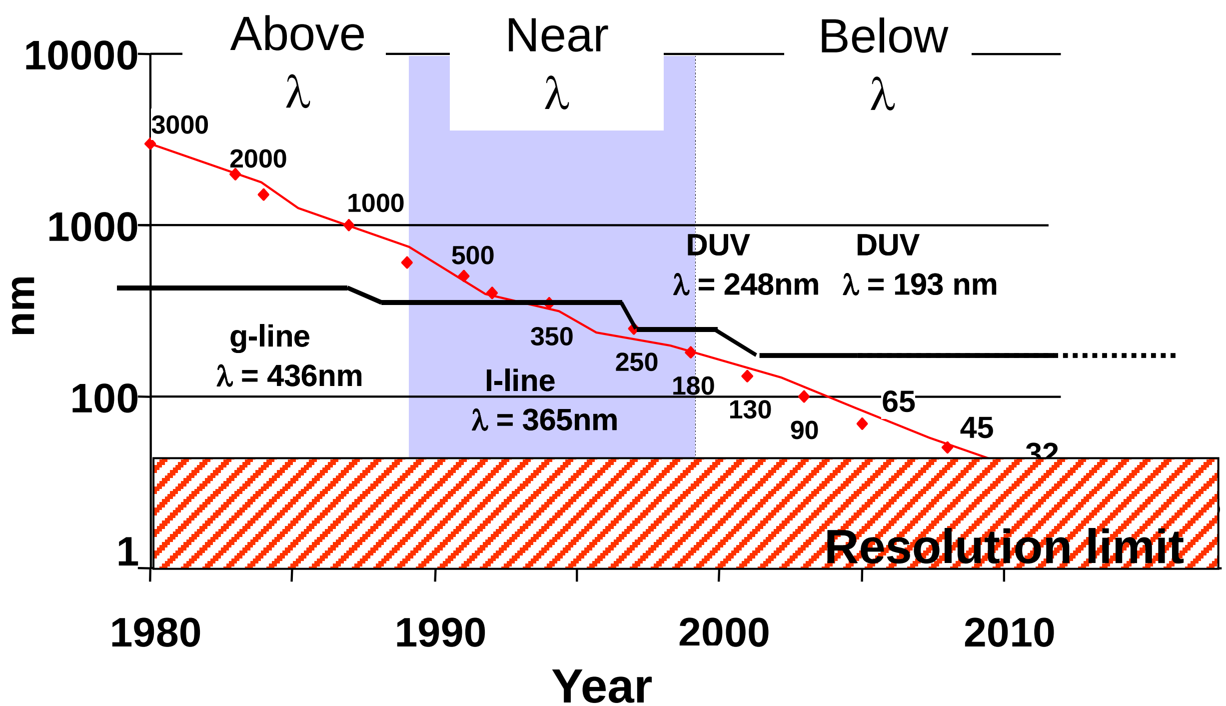
Resolution improvement?

$$R = k_1 \times \frac{\lambda}{NA}$$

Ultimate k1: 0.25 (simple exposure)





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Discussion on k1 improvement

- Resist process concern
- Illumination improvement
- OPC solution

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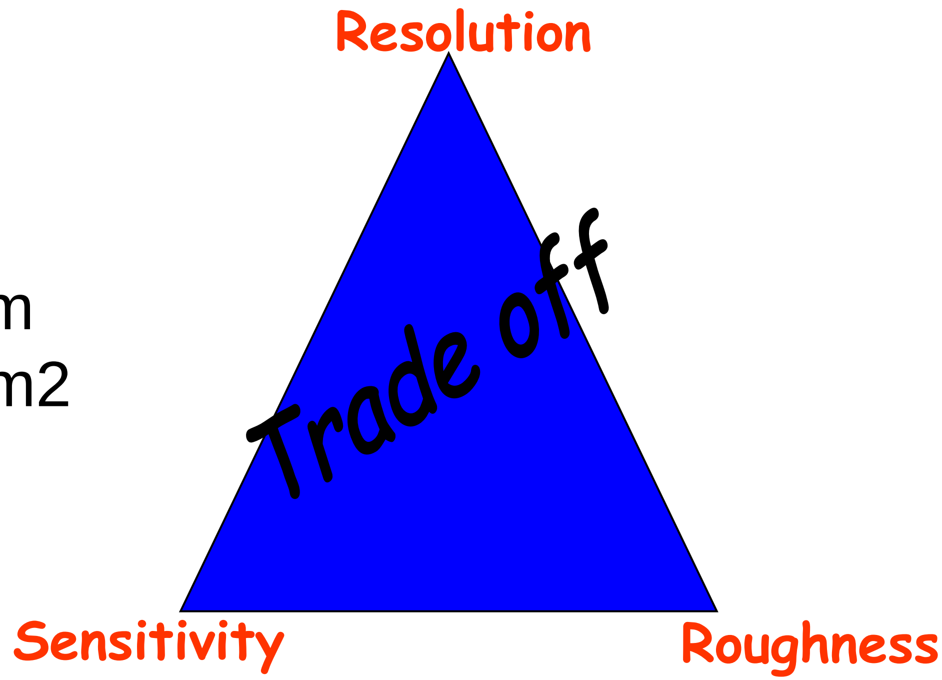
Resist process concern

Today's challenges

- ➢Resolution sub 20 nm
- ➢Sensitivity ~10 mJ/cm2
- ➢ Roughness < 2 nm



But also:

- ➢Etching selectivity
- ➢Adhesion and Mechanical stability (pattern collapse)
- ➢Thermal stability (resist flow)
- ➢Chemical stability (shelf life)
- ➢ Purity (defects, metallic contamination)

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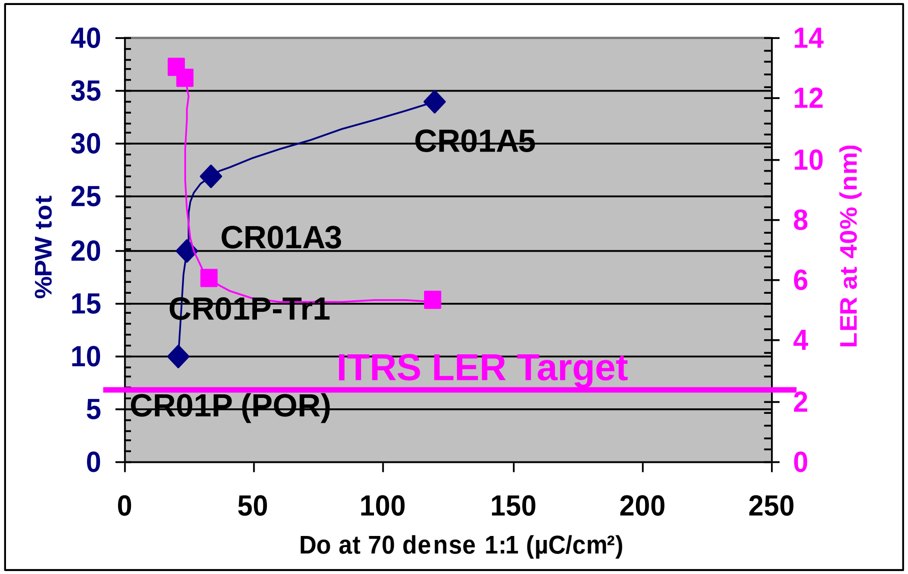
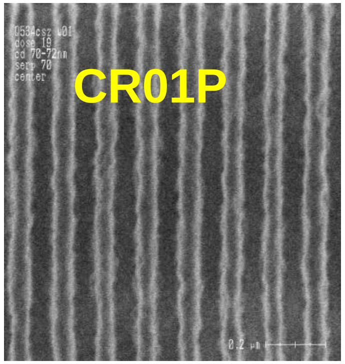
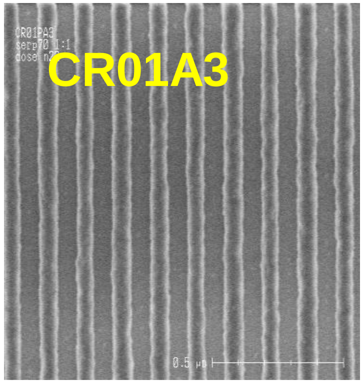
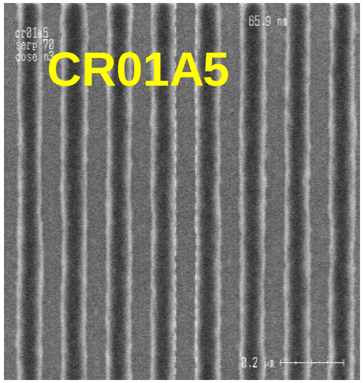
Sensitivity impact

- Trade-off requirement between sensitivity/LWR/Process window









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Discussion on k1 improvement

- Resist process concern
- Illumination improvement
- OPC solution

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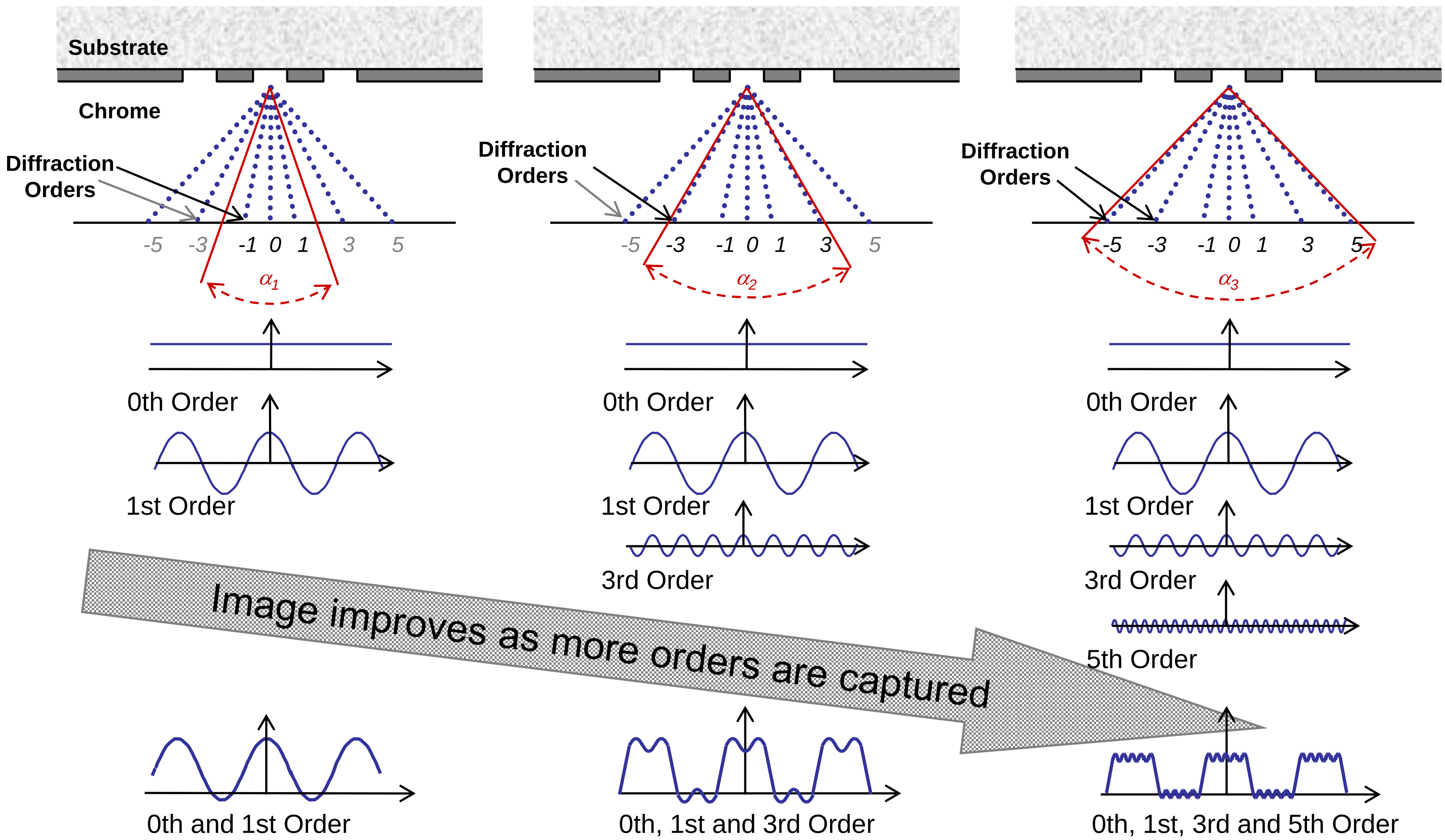
Image Capture



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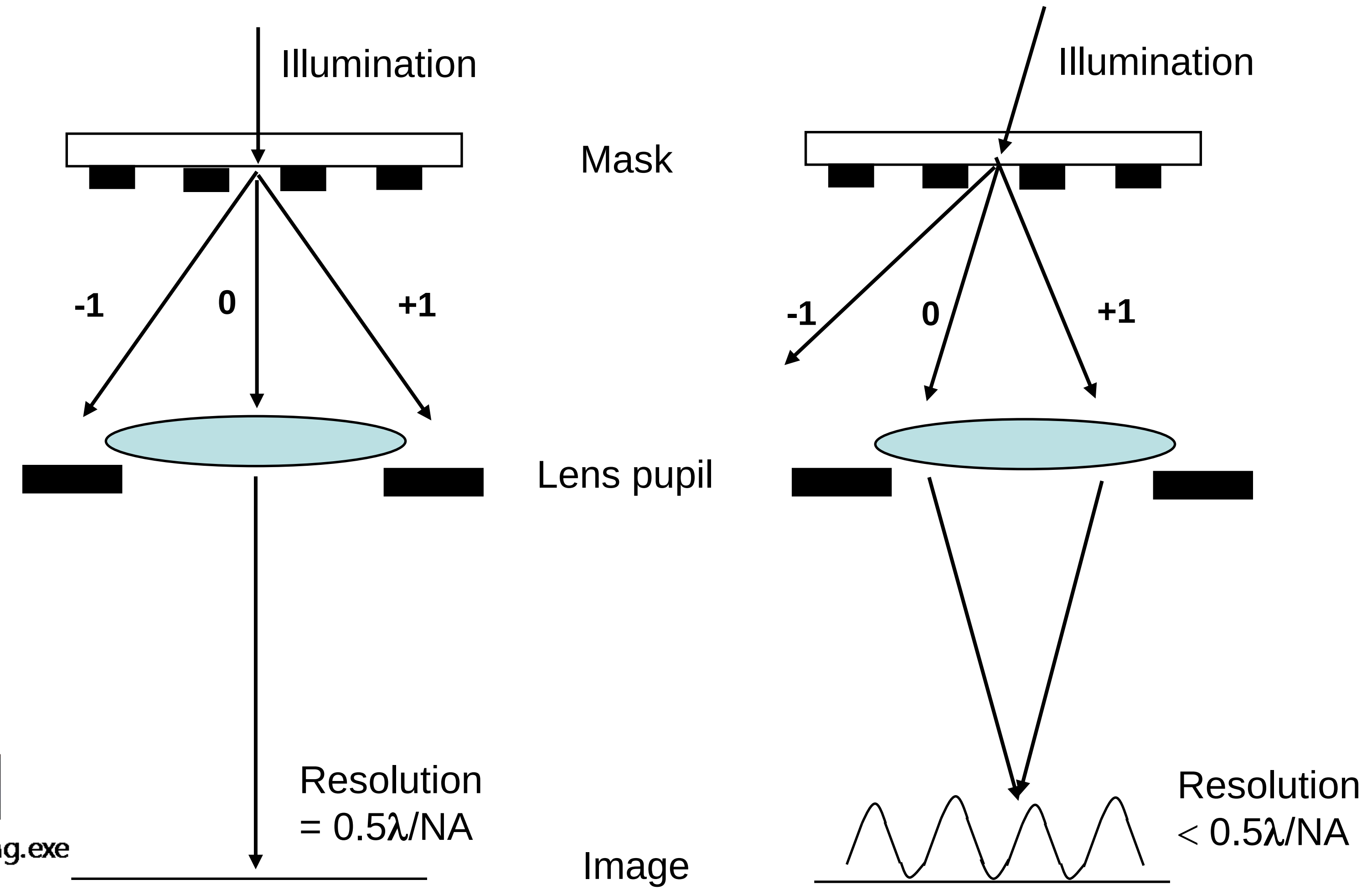
Optical Engineering: OAI

- Primarily used for improving resolution/DOF of dense features



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Discussion on k1 improvement

- Resist process concern
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- OPC solution

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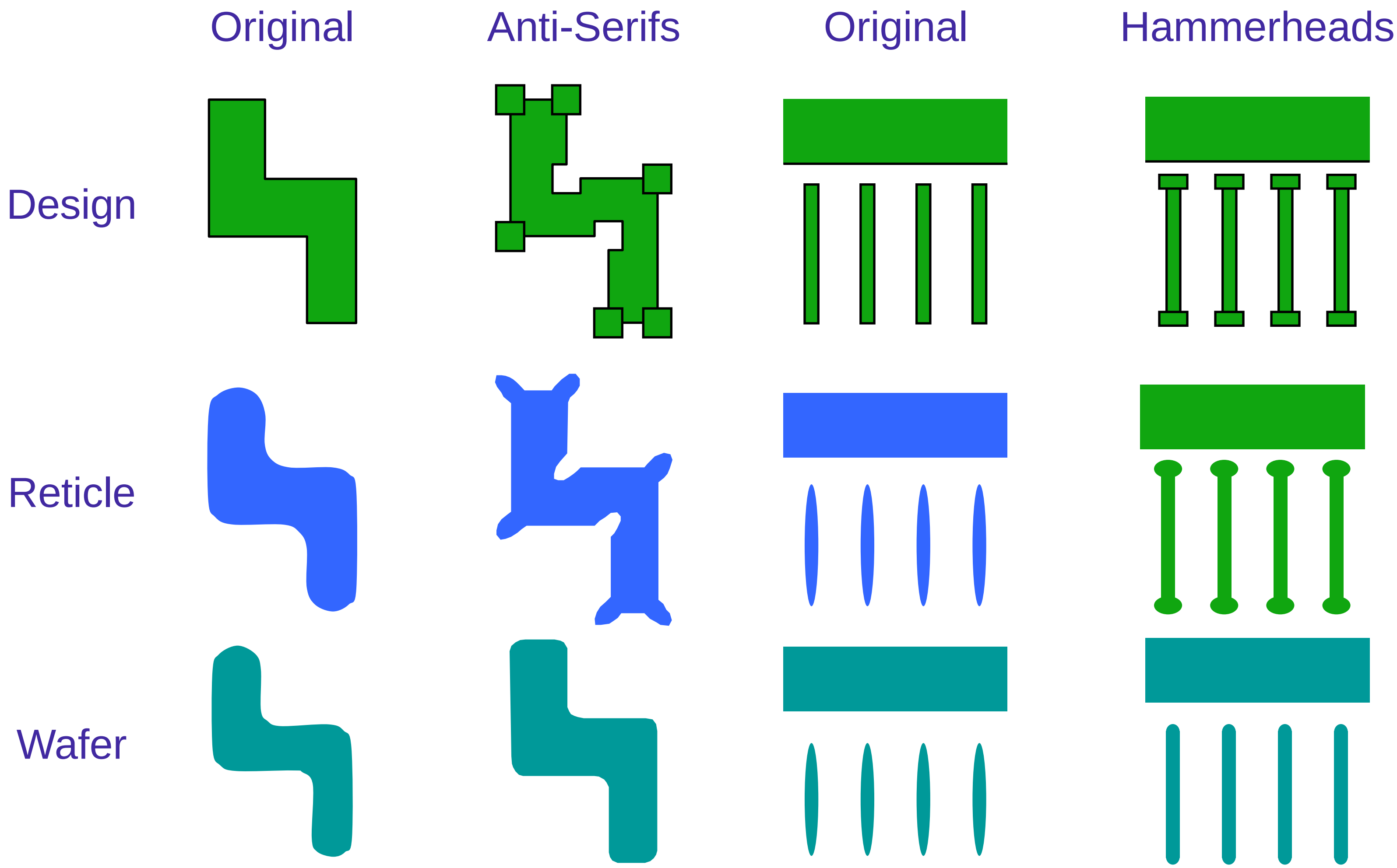
Optical Engineering: OPC



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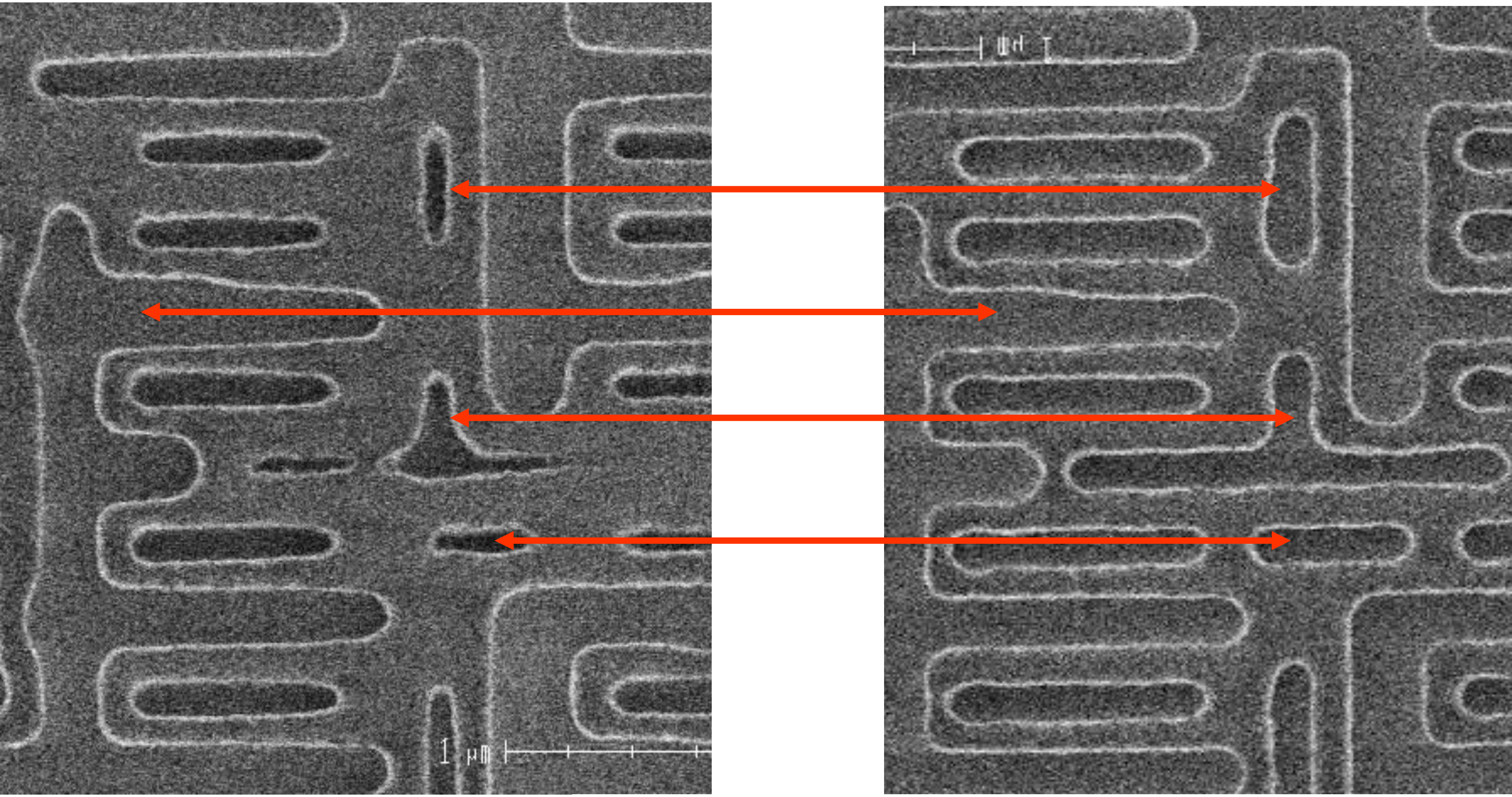
Optical Proximity Correction (OPC)

No OPC C065 Metal1 **OPC**



Courtesy of Y. Trouiller

Hardware for OPC

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Lithography options for tomorrow

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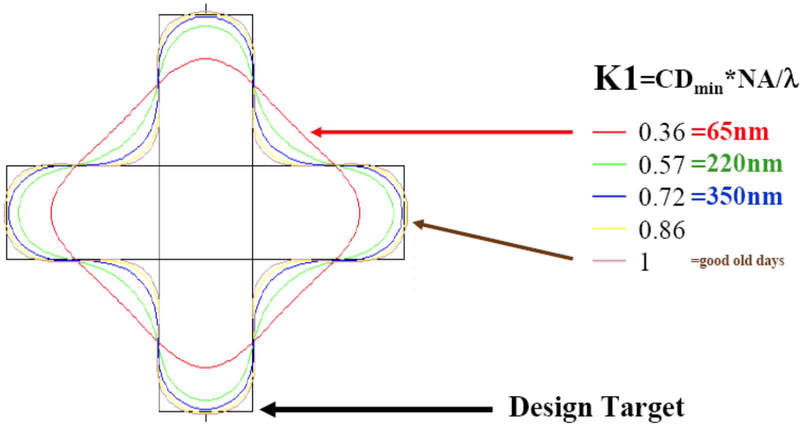
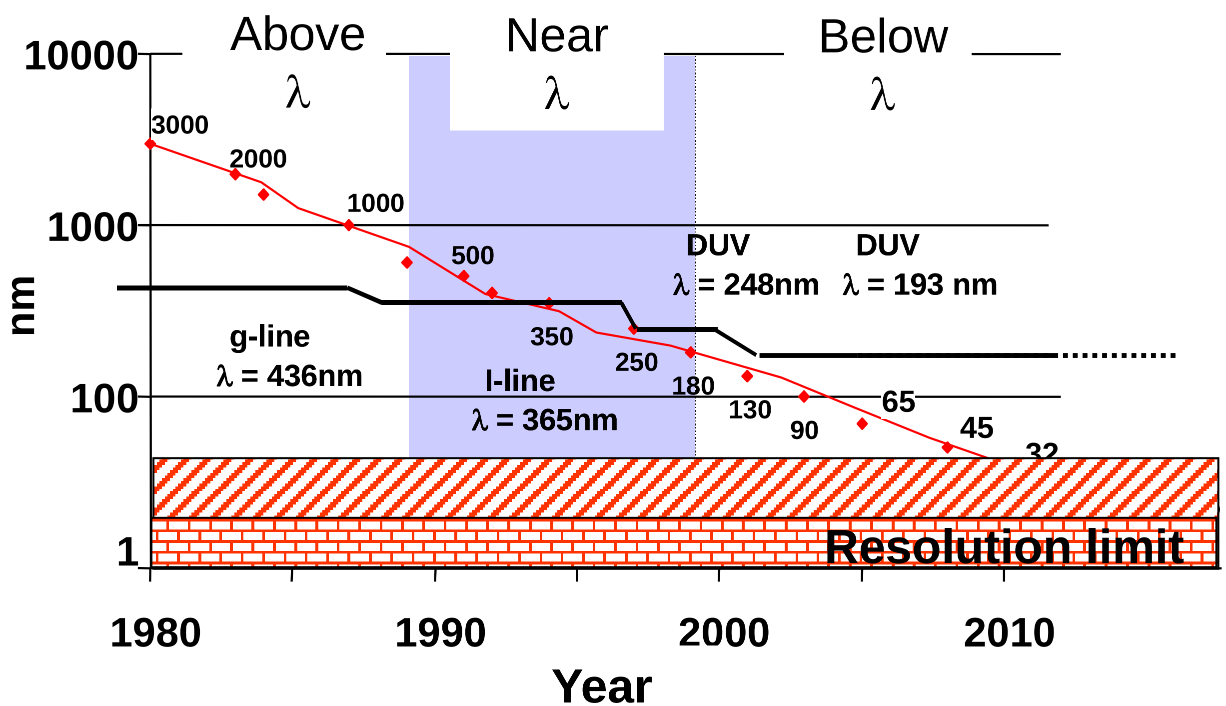
Ultimate resolution?

$$R = k_1 \times \frac{\lambda}{NA}$$



Ultimate k1: **0,22** (*double* exposure)



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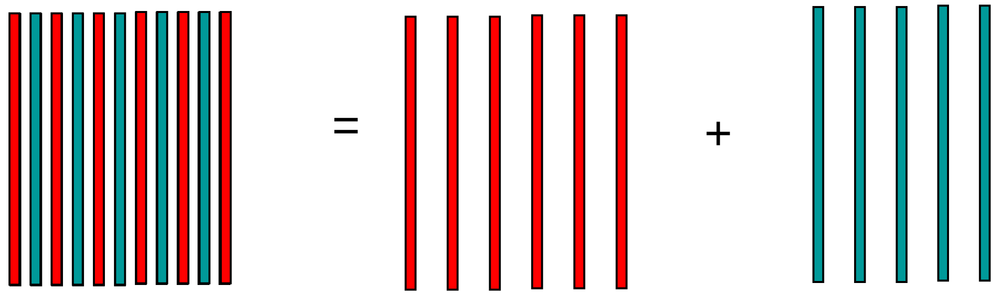
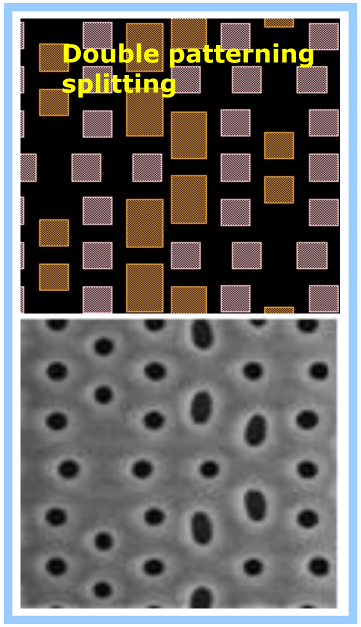
How to push again 193nm lithography? Double exposure technique – option 1

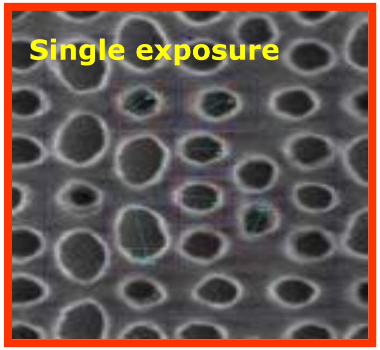
- 2 exposures → to resolve most agressive pitches



KEY ADVANTAGE

Resolution



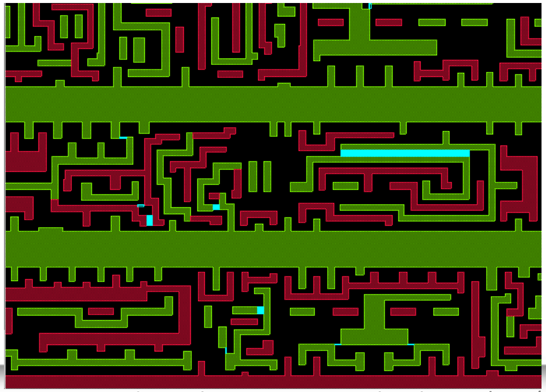


CHALLENGES

Technological cost

Alignment

Design decomposition



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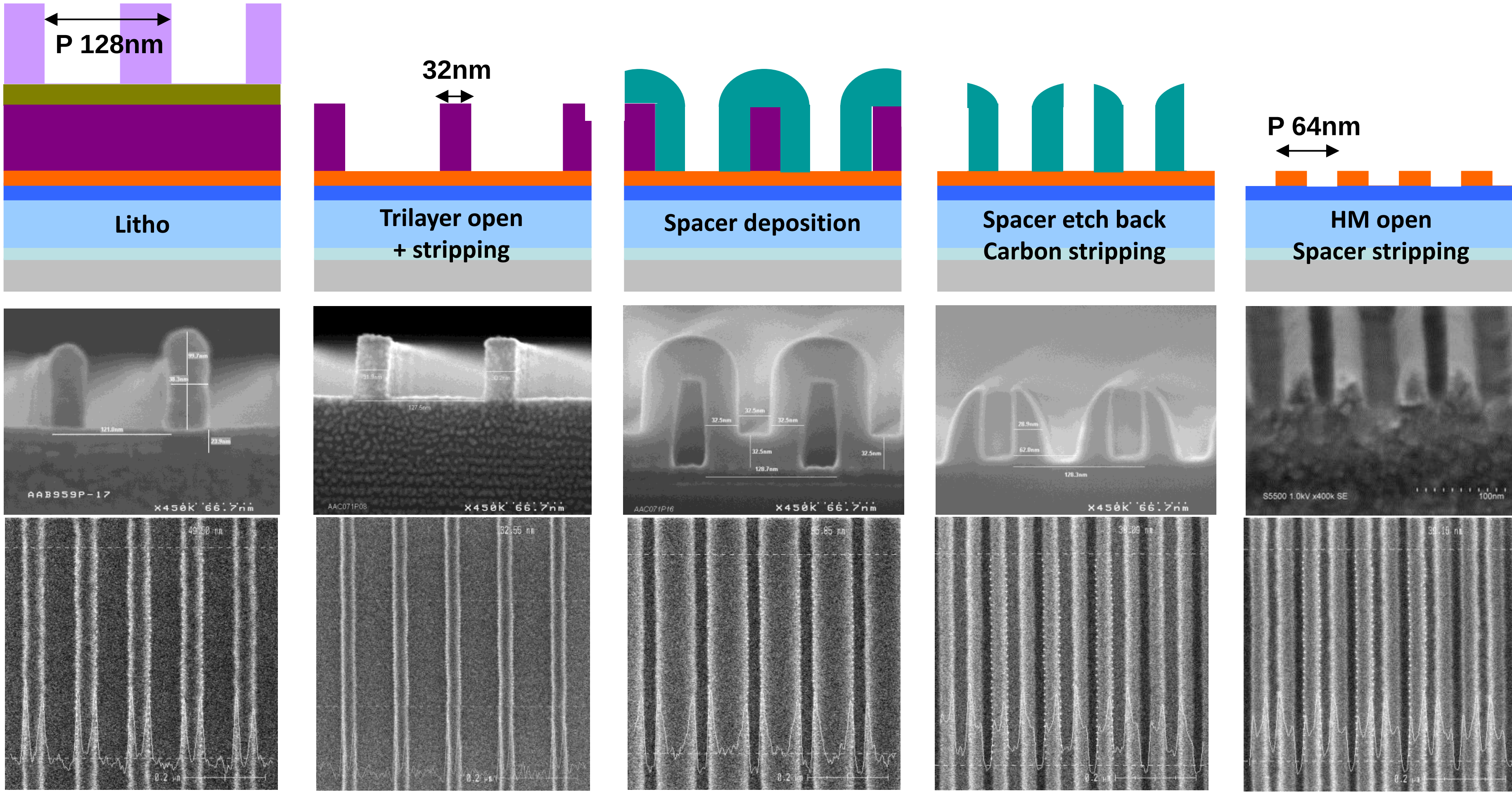
Double exposure– option 2
Pitch doubling



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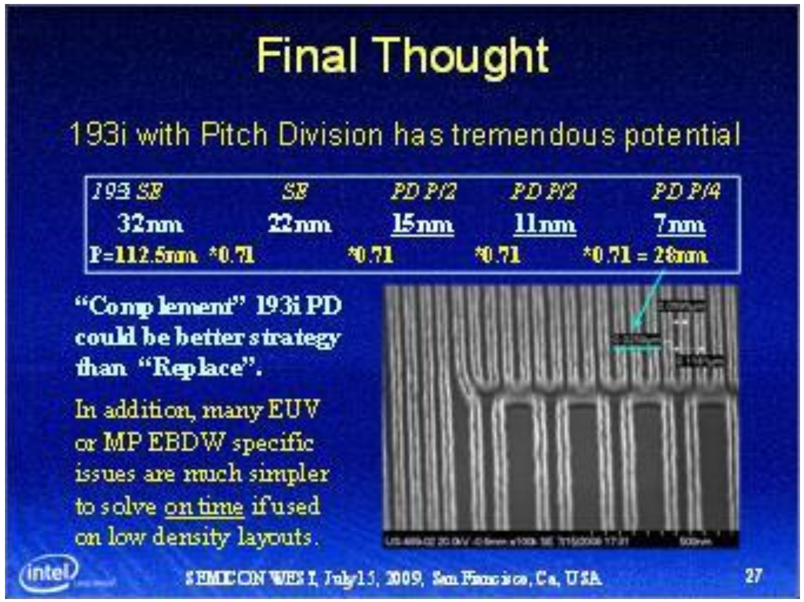
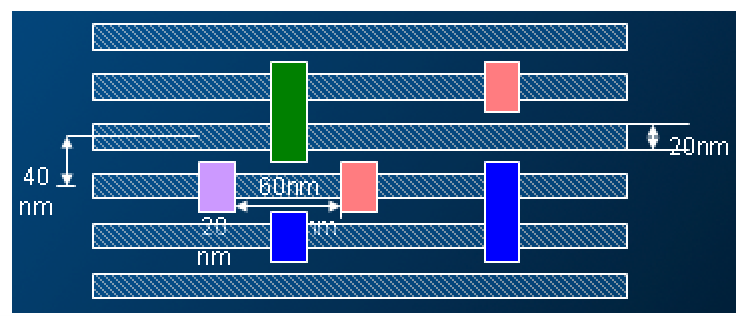
+/- SADP process flows

- The big **PLUS** : long term extendibility



- Minus
  - Technological cost
  - Complexity :
    - Spacer control
    - 2nd exposure…
    - Design rules



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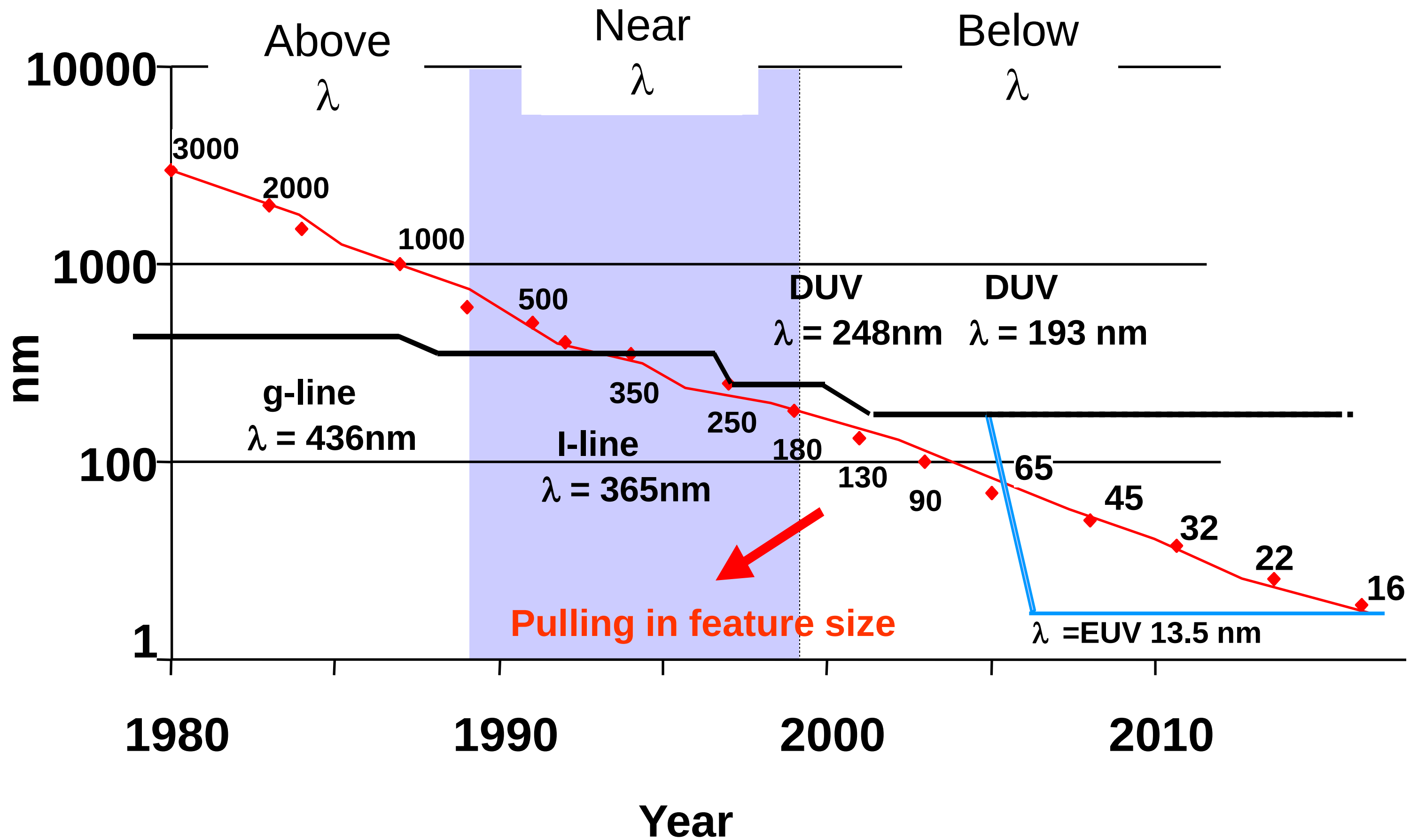
$$R = k_1 \times \frac{\lambda}{NA}$$

EUV lithography
The next optical generation?

Return to high k1 regime…



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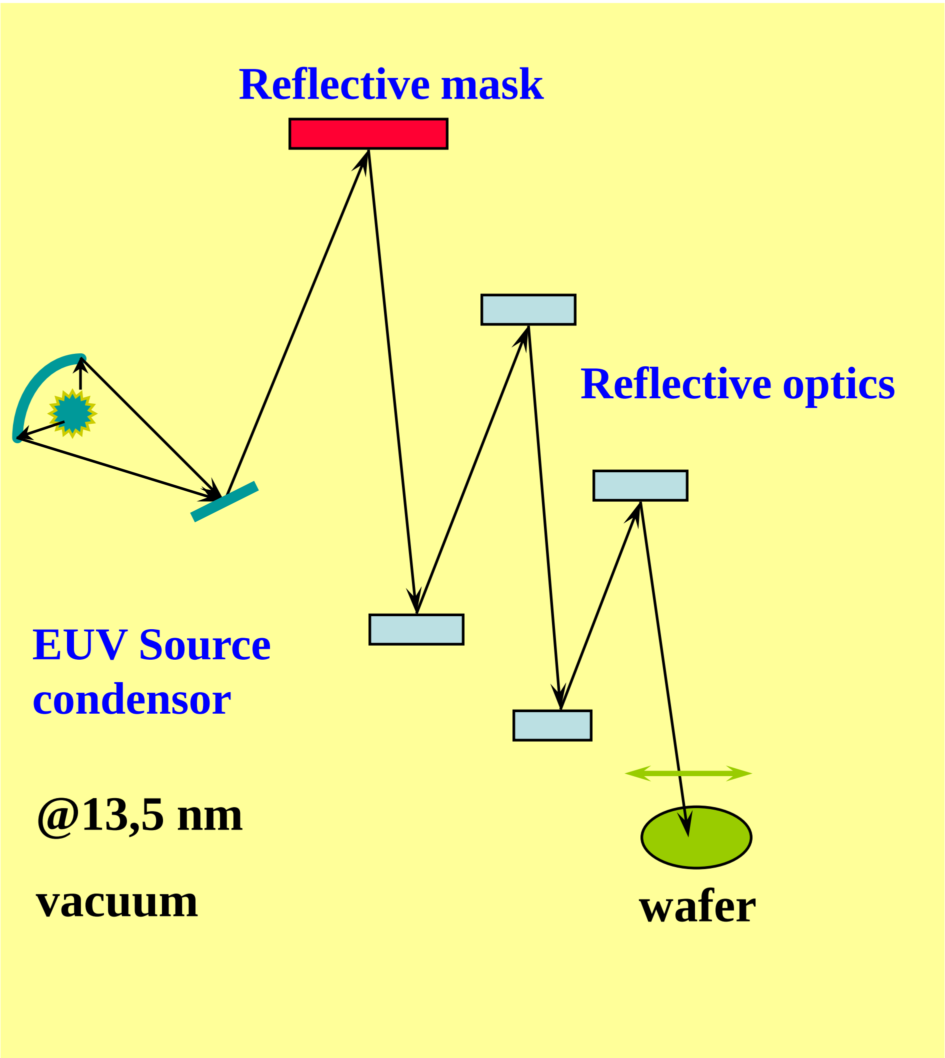
Les challenges de la lithography EUV?



Absorption problematic

- ✓Vacuum
- ✓Mask & reflective optics

Sources: power

- ✓Target : 250W min… up to 1kW
- ✓Stability
- ✓Debri residus

Specifications

- ✓ML mirrors: 70% reflectivity
- ✓Masks: defects< 10^{-3} defects/cm^2
- ✓optics: < 0.1 nm roughness

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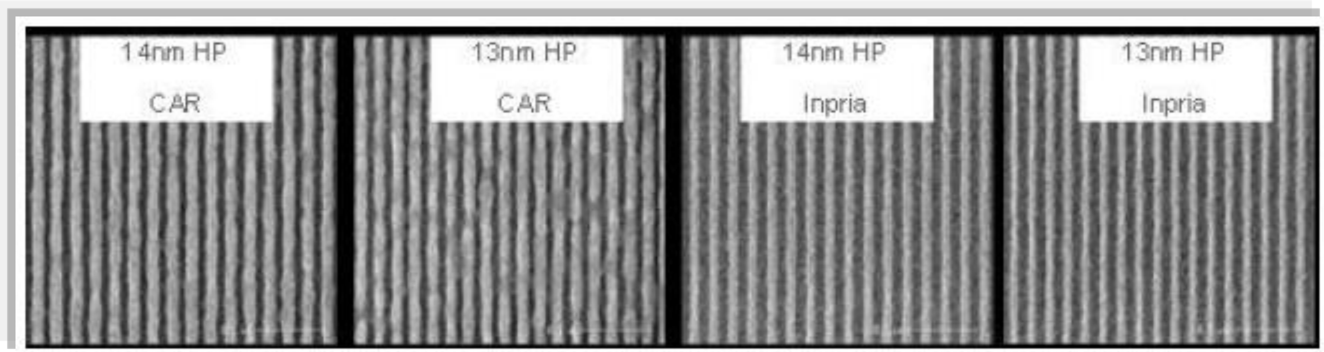
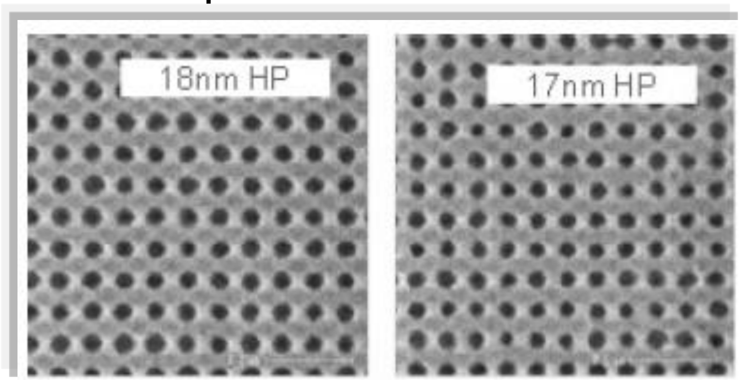
Performances



Line & space CAR and non CAR
Dipole illumination



Contact CAR
QUASAR illumination

R Peeters, Proc. of SPIE Vol. 8679 86791F-5 - 2013

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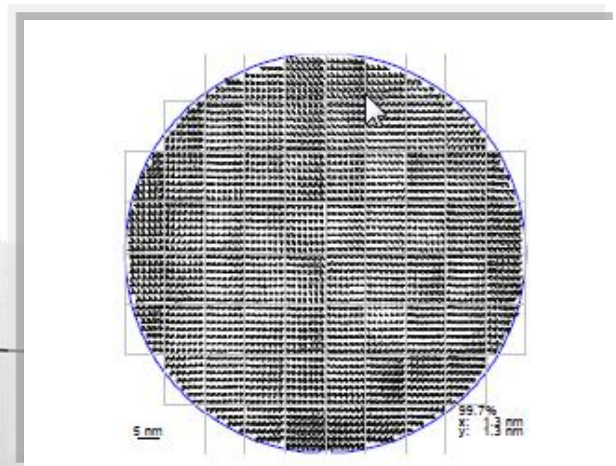
1st indu… latforms ready

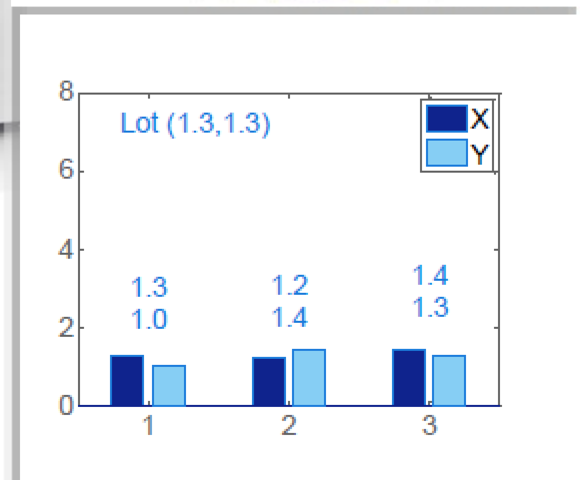
NXE: … H1 2012

2n… raised to 0.33NA

CHALLENGES

Source power
Need 250W → Today up to 50W/1h
Mask infrastructure not ready
resist → need sensitivity improvement
Technology cost → litho cell around 250M$





	NXE:3100	NXE:3300B
NA	0.25	0.33
Illumination	Conventional 0.8 σ	Conventional 0.9 σ
Resolution	27 nm	22 nm
Overlay DCO/MMO	4.0 nm / 7.0 nm	3.0 nm / 5.0 nm
Productivity	60 Wafers / hour	125 Wafers / hour
Resist Dose	10 mJ / cm2	15 mJ / cm2

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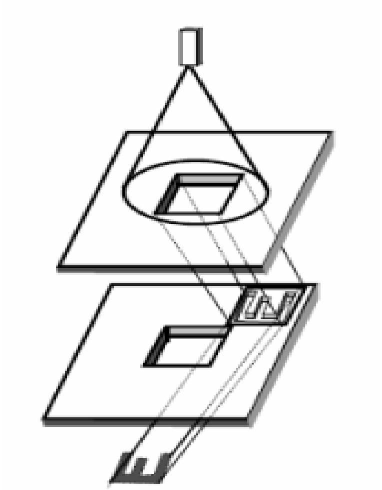
Electron beam direct write lithography

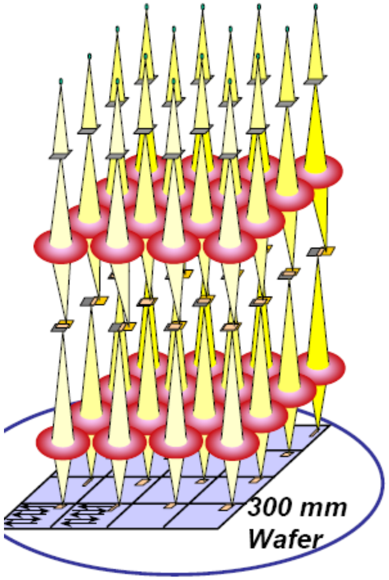
- A mature technology… since 1960!
  - High resolution capability → λ = 0.004 nm @100keV
- Several options

Single beams



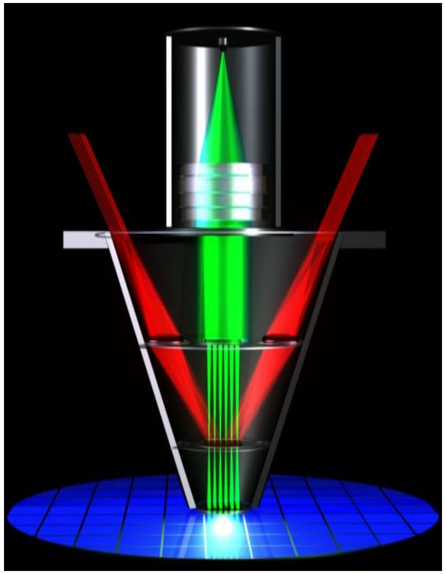
→2-5w/day
→R&D

Multi-columns



→1pl/2-5h
→Small serie

Multi-beams



→10w/hour
→Production

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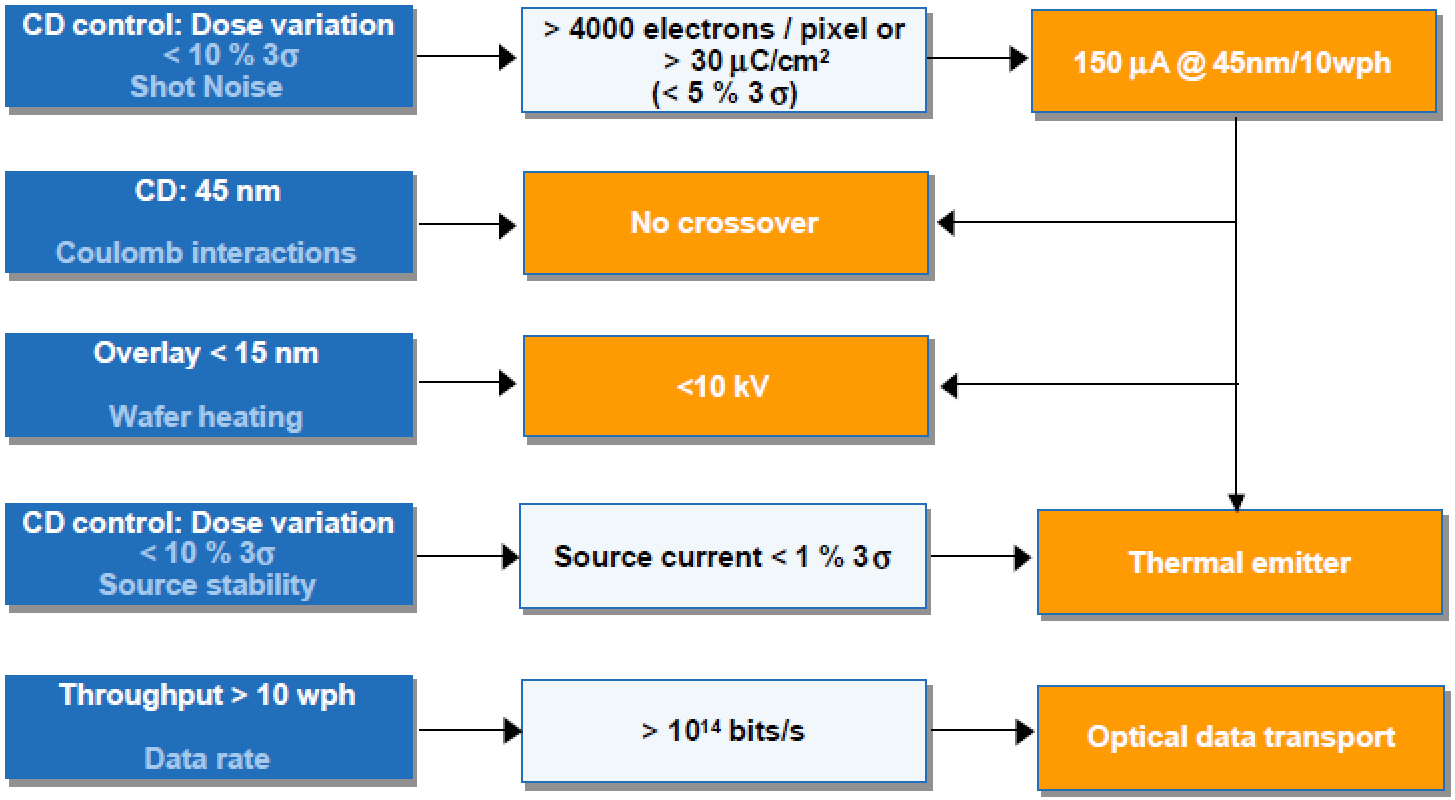
How to build a multibeam machine?

Design constraints

To meet the 45 nm (hp) specs @ 10 wph, several constraints apply…



MAPPER workshop – Delft Sept 2005

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Machine specifications

MAPPER Lithography

Design constraints

… which drive the system parameters

150 µA @ 45nm/10wph →	Brightness: Highest available thermal emitter < 10^7 A/m²SrV →	> 13,000 beams required
No crossover →	13,000 e-beam columns →	13,000 lenses without individual control
<10 kV →	Electron scattering →	Existing bi-layer resist
Thermal emitter →		Existing single source
Optical data transport →	7.5 GHz per data channel →	Existing telecom technology

MAPPER workshop – Delft Sept 2005

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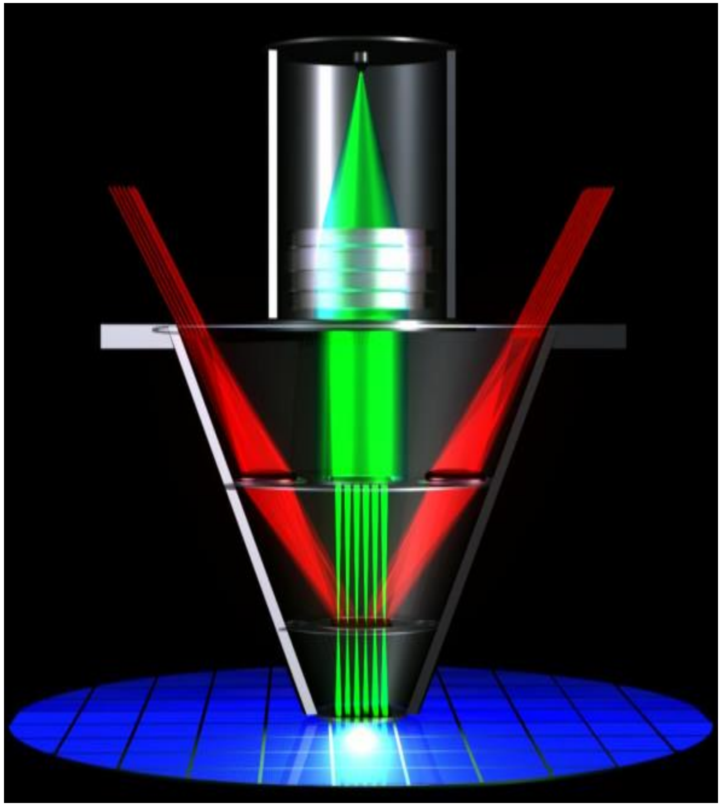
MULTIBEAM CONCEPT
The MAPPER technologie

- A movie to understand the principle



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MULTIBEAM
Benefits and doubts

- Benefits
  - Resolution/Flexibility
  - Economical gain
  - Industrial capability
  - Industrial compatibility

- Doubts
  - Industrial maturity
    - Technology maturity
    - Timing for industry
    - Strong industrial partnership & commitment
  - Data treatment (speed & integrity)
  - Infrastructure

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MAPPER production tool roadmap

	FLX-1200/800 Available Q2 2014			FLX 1200T/800T Available Q32015		
Imaging						
technology node	65nm	40nm	28nm	65nm	40nm	28nm
Throughput						
WPH 300mm	2	2	1	5	5	2.5
WPH200mm	4	4	2	10	10	5
Overlay						
single machine	10nm			10nm		
Field size						
max x	26.0mm			26.0mm		
max y	33.0mm			33.0mm		
UDOF	200nm			200nm		
Data inut format	OASIS.MAPPER			OASIS.MAPPER		

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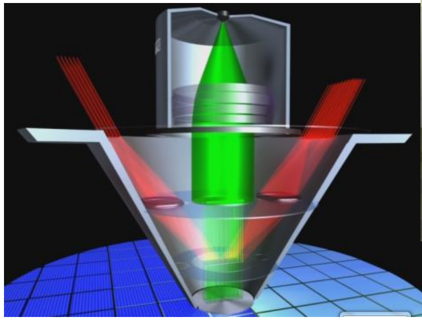
LETI – MAPPER IMAGINE consortium



How to support MAPPER up to industrial technology take off

1 module
1 → 10wph

10 clustered modules
10wph/module

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Consortium outlook

SOKUDO ✓ TEL ✓ Canon ✓

Nissan Chemical ✓

tok ✓

DOW ✓

JSR Micro ✓

tsmc ✓

ST ✓

Imagine

Mentor Graphics ✓ aselta NANOGRAPHICS ✓

✓ Participation renewed for 2013

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IMAGINE environnent

PLATFORM ASSESSMENT

Technology assessment
Qualify MATRIX generation

EPC

Get tool format concensus
Validate data flow
Qualify EPC strategy

PROCESS

100% resist partner tests
Push process capabilities

OUTGASSING

Test resist partners
Work on contamination

INTEGRATION

Demonstrate CMOS process flow compatibility

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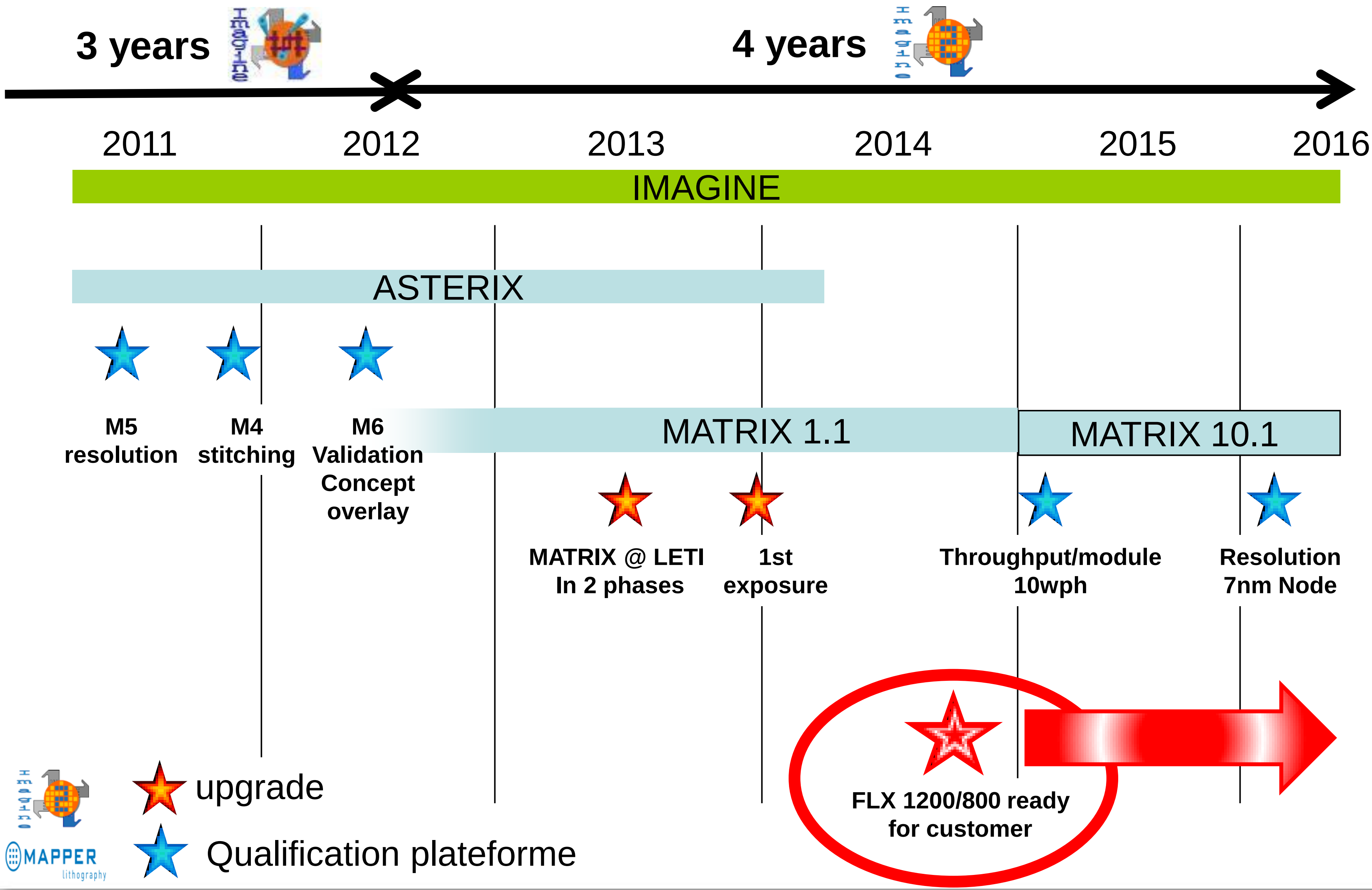
IMAGINE roadmap



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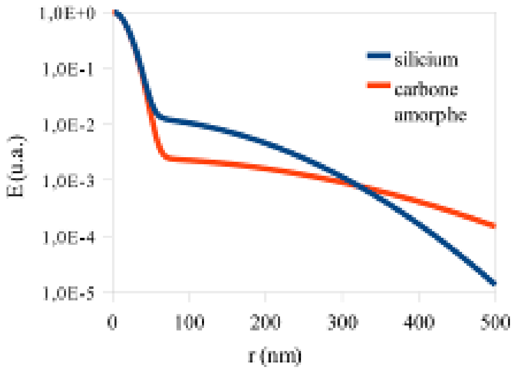
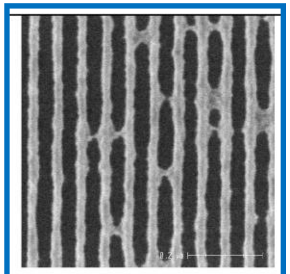
Reference process baseline

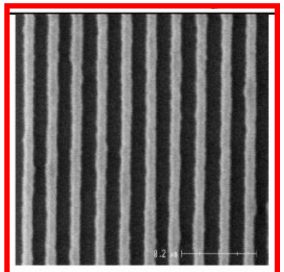
1. Resist stack

1. Optimized to decrease backscattering electrons at 5keV
2. Compliant with CMOS process → use of tri-layer process stack





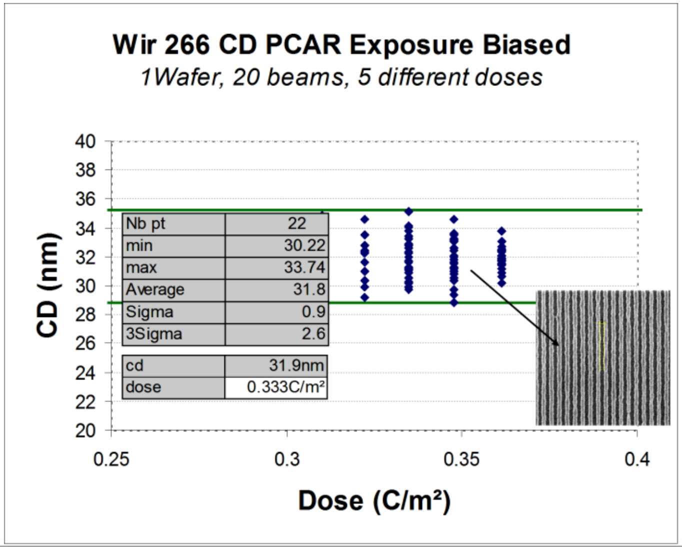
$D = 357\mu C/cm^2$
$CD = 23nm$
$LER = 7,5nm$

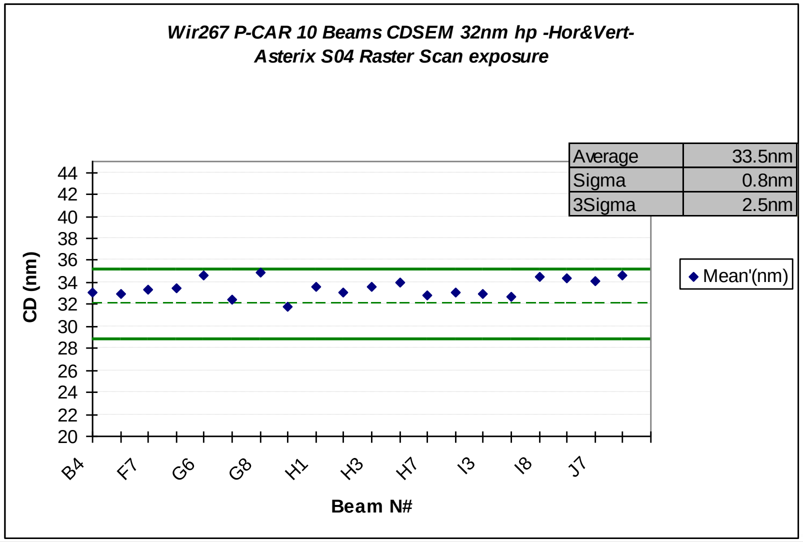


$D = 673\mu C/cm^2$
$CD = 22nm$
$LER = 4,9nm$

HSQ

2. 32nmhp capability on p-CAR (PoR)





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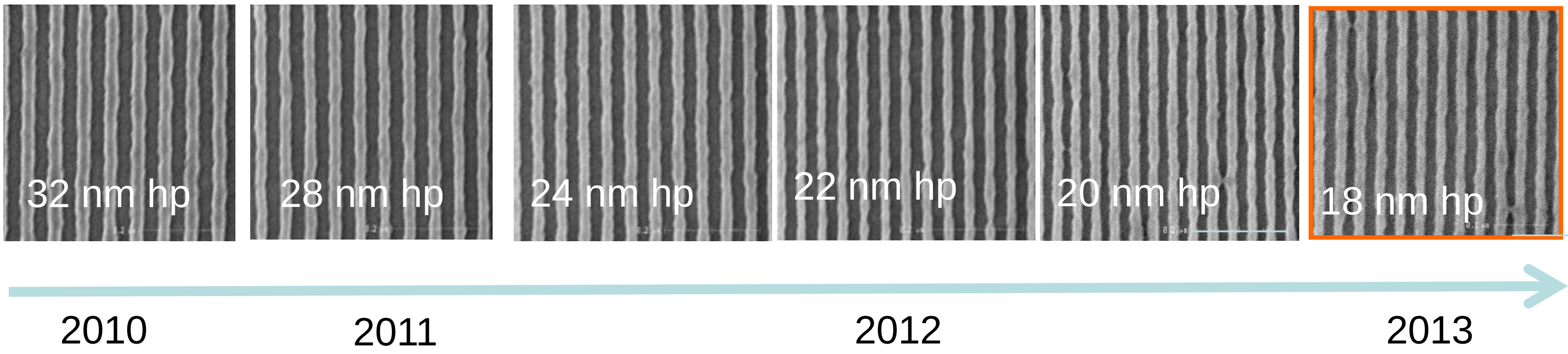
1st steps on technology learning
Prototype platform feedback

- Learning on preventive maintenance plan
  - Main Illumination Optic (MILO) swap on quarterly basis
  - Projection Optic System (POS) upgrade
  - Stage instabilities : sensors, knife edge

- Regular progress on resolution performances



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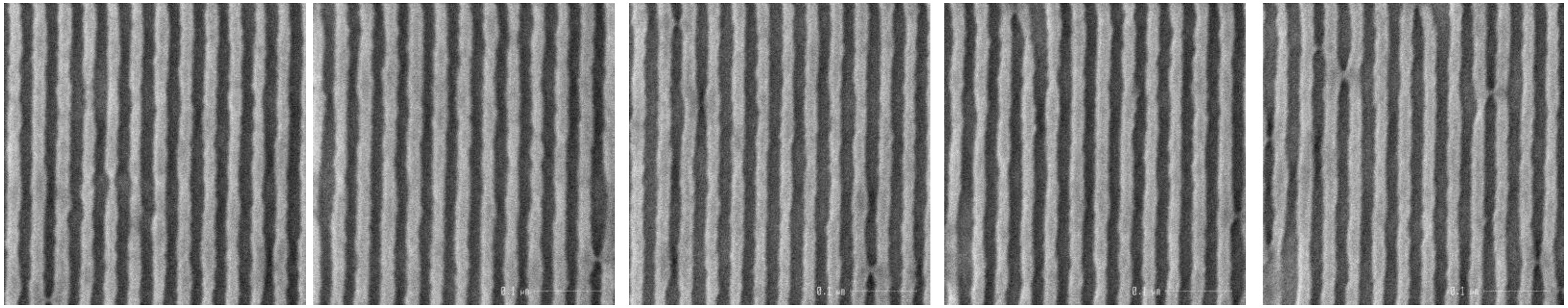
Best resolution with PoR

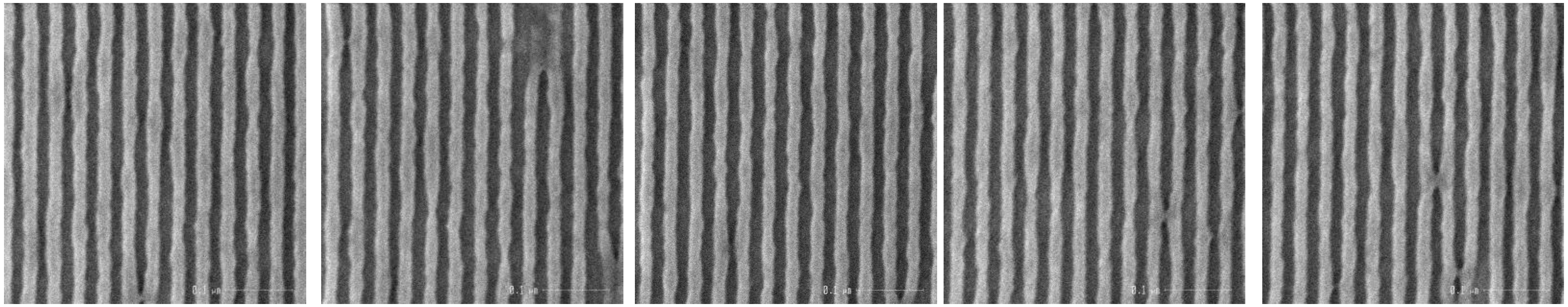
Prototype S04 Champion resolution
Latest results with PoR

18nm hp



F6 Beam F7 F8 F9 F10

D=80 µC/Cm2



G1 G3 G5 G7 G9

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LETI process capability improvement

- 2 new 300mm tracks arrived in Q4 2012
  - R&D configurations to address advanced process developments
    - Multibeam
    - DSA
- Installation in progress
  - SOKUDO DUO : SAT completed
  - TEL Lithius : under acceptance (almost completed)


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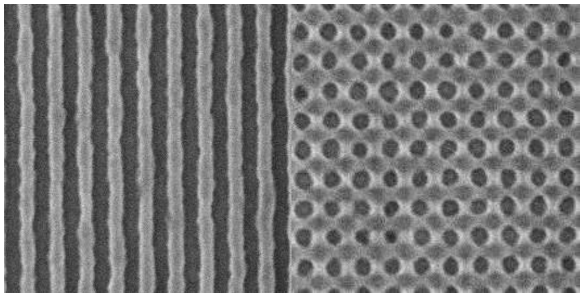
Resist sensitivity status

- Resist sensitivity on target @ 5kV for 20nm node

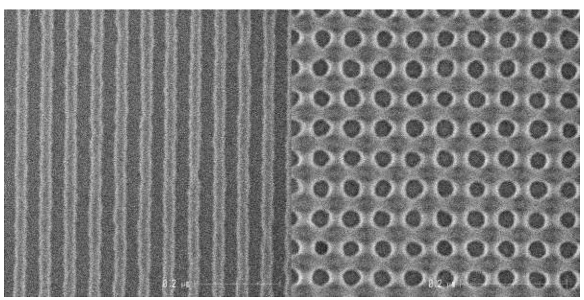
5kV
28nm dense
L/S & Contact

A



D0=20µC/Cm² D0=36µC/Cm²

C

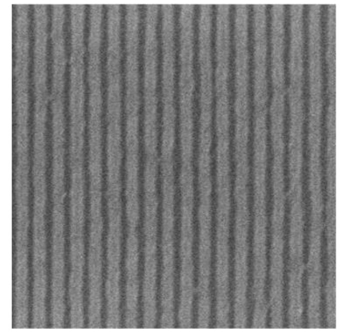


D0=30µC/Cm² D0=61µC/Cm²

100kV

19nm

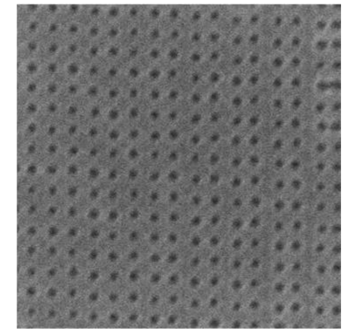
Test Resist A



460uC/cm²

15nm

Test Resist B



660uC/cm²

LS design	Dose to size (µC/cm²)	Expo latitude (µC/cm²/nm)	LWR
32/64	29	0.37	4.4
28/56	30	0.27	4.6
24/48	-	-	-
12/48	59	0.93	4.2

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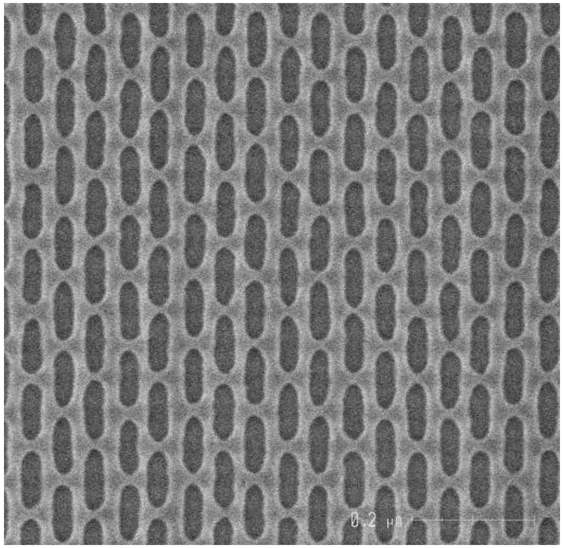
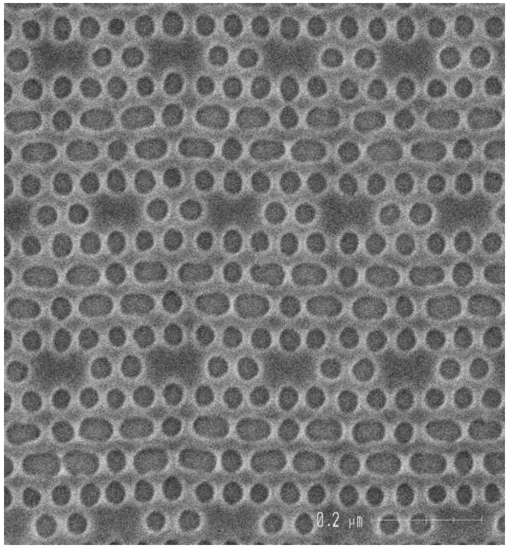
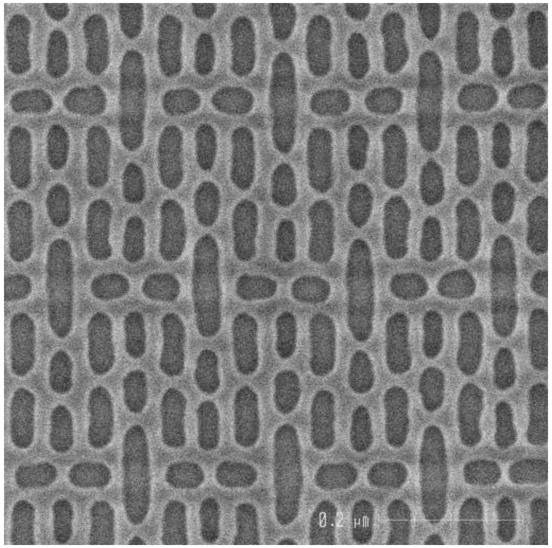
Resolution demonstration



Brickwall 26nm hp
CD 26nm

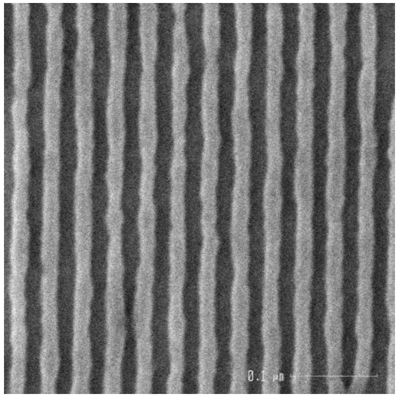


Contact 24nm hp
CD 26nm

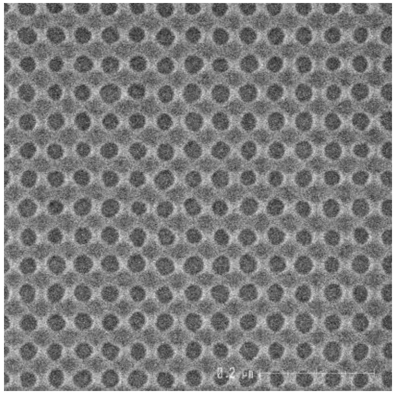


Metal 1 24nm hp
CD 26nm

MAPPER



18nm hp



22nm hp

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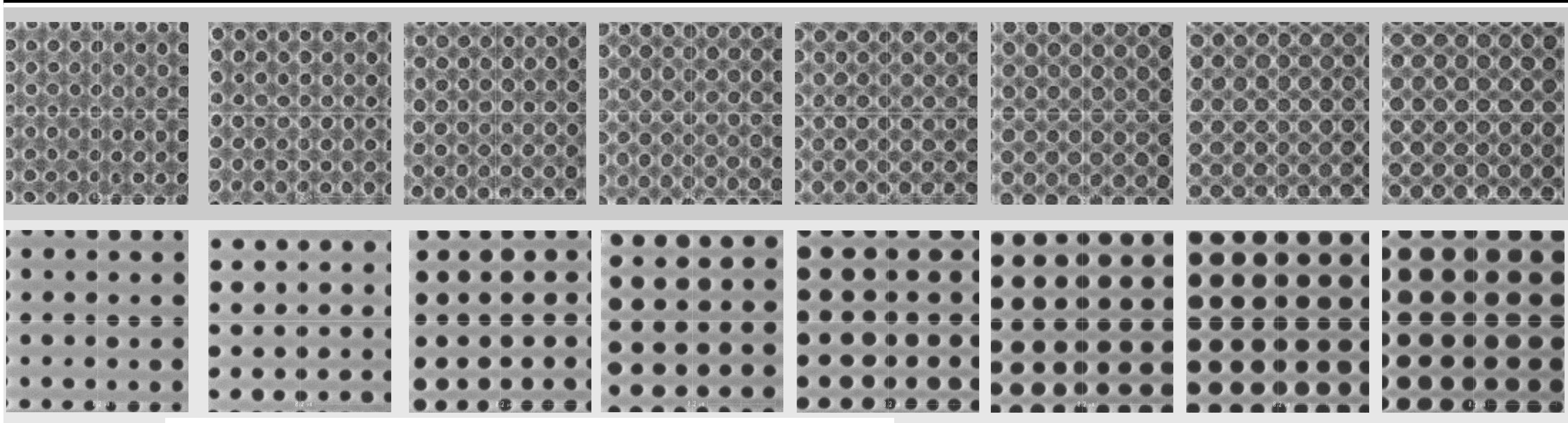
Etch demonstration

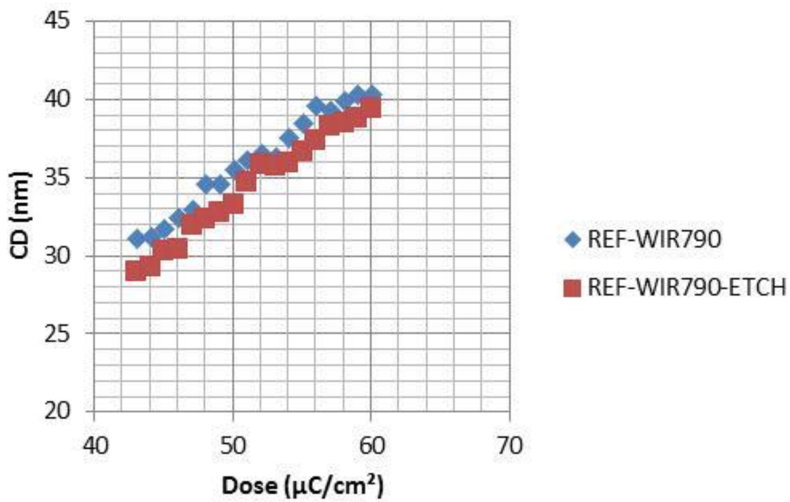
CONT 32-Pitch 64nm

45µC/cm²	47	49	51	53	55	57	59

AFTER LITHO

AFTER ETCH





SiArc+SOC open with standard LETI etch chemistry

CD contact <u>-1.5nm</u> after etch

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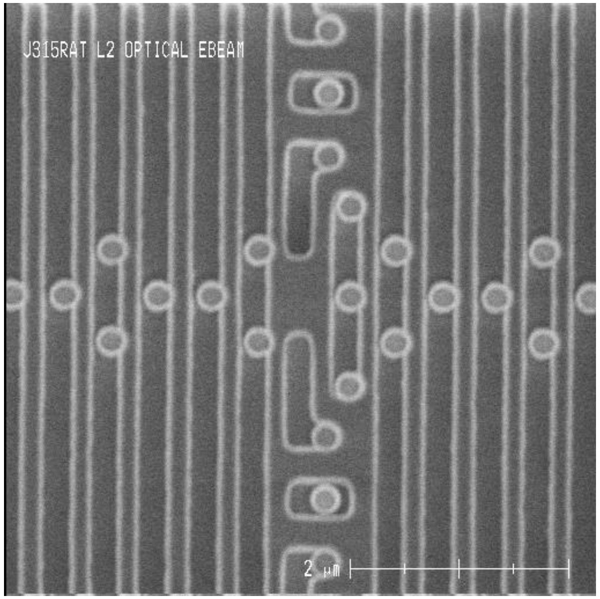
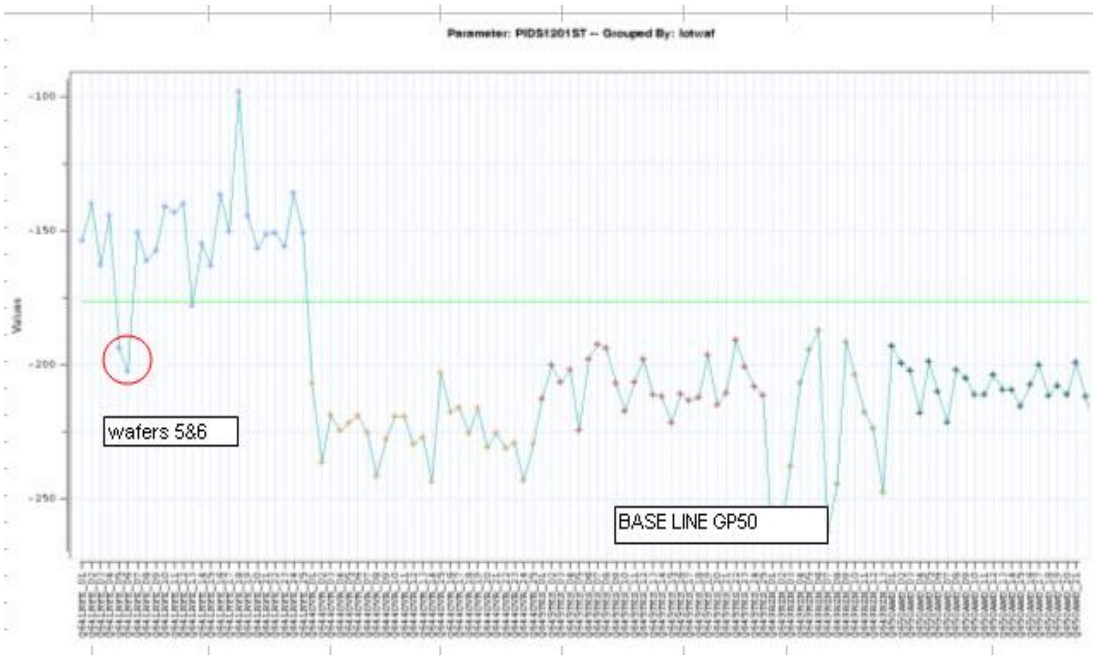
EBDW processes integration capability

- Several demonstrations done using single beam systems
  - No issue with 50kV systems : No technical issue – No resist thickness constraint
  - Electrical results aligned reference optical lot

Via1 : optical
Metal2 : E-Beam



Implant level
EBDW corner lot vs. optical reference
On CD mismatch



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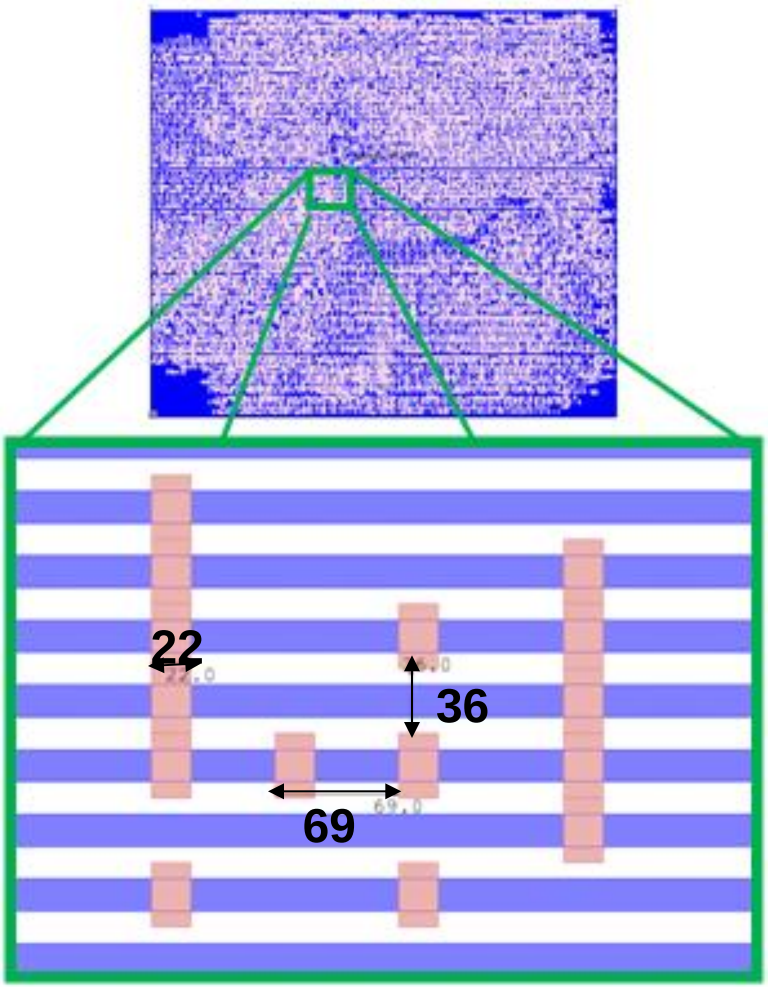
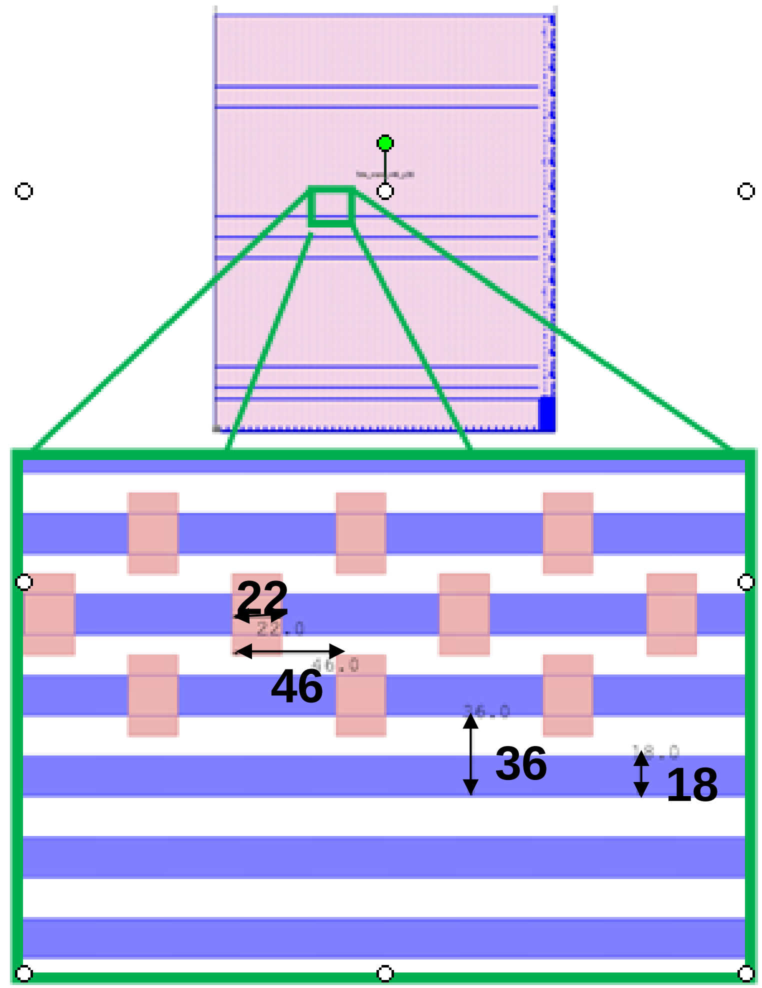
Case of 5kV – Litho cut - 36nm pitch Layout

Logic block



SRAM block



Tela Innovations

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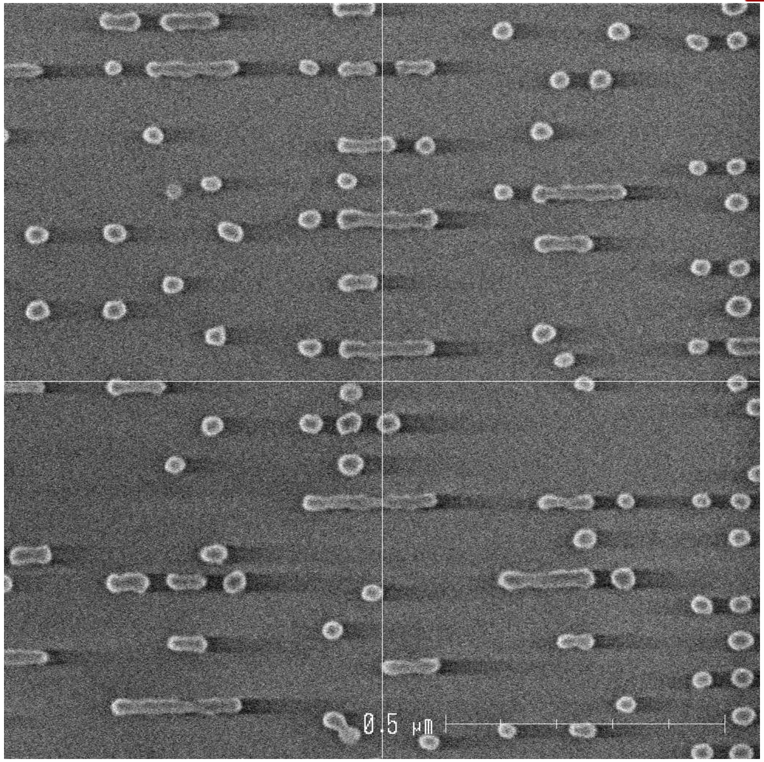
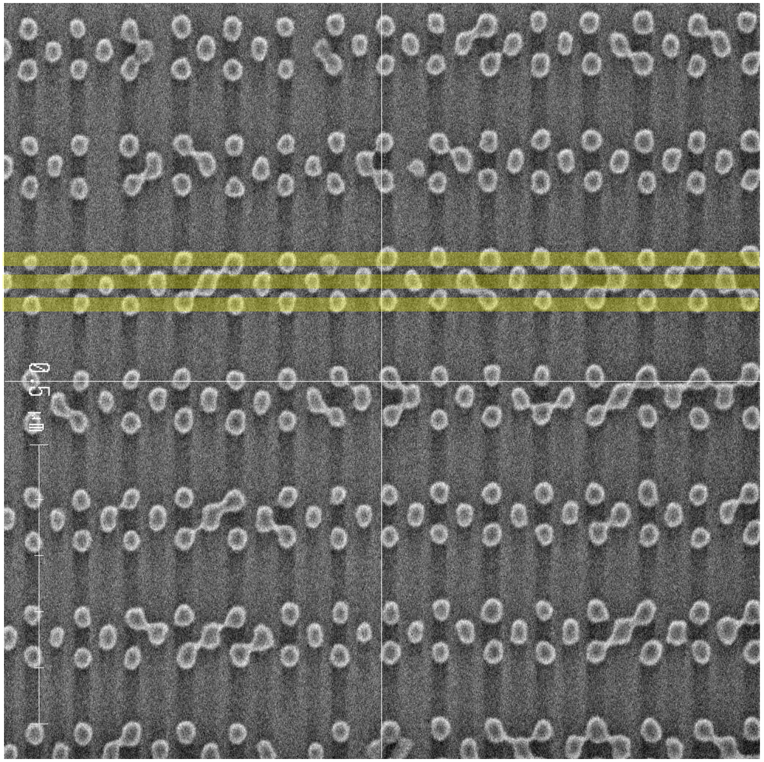
36nm pitch Layout with MAPPER platform

Logic block



SRAM block



Positive tone: 90% density

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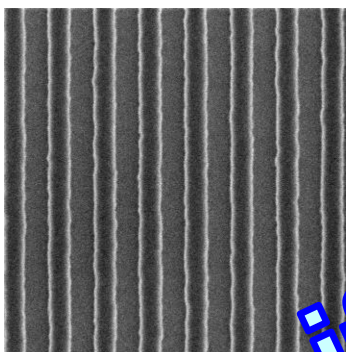
Focus on resolution for 90 & 65nm node

- Resolution & high throughput potential

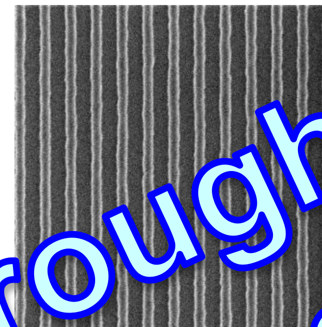
C065



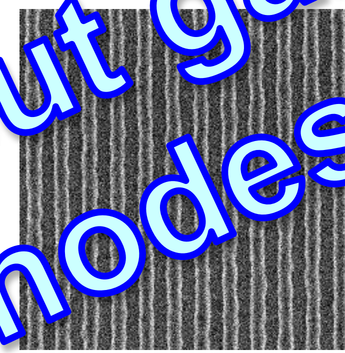
pCAR - 12µC/cm²

nCAR - 8µC/cm²

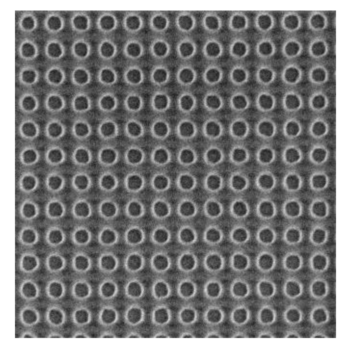
C045



pCAR - 14µC/cm²



nCAR - 8µC/cm²



pCAR - 18µC/cm²

Significant throughput gain wrt to advanced nodes

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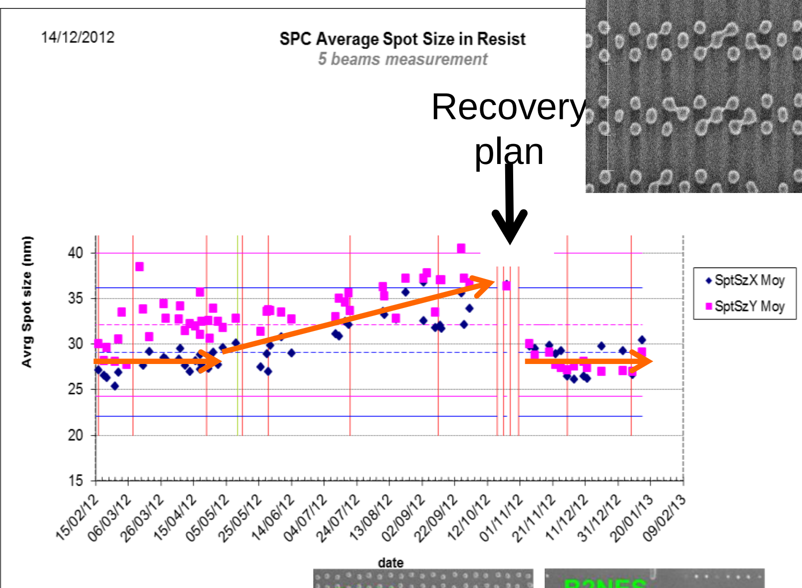
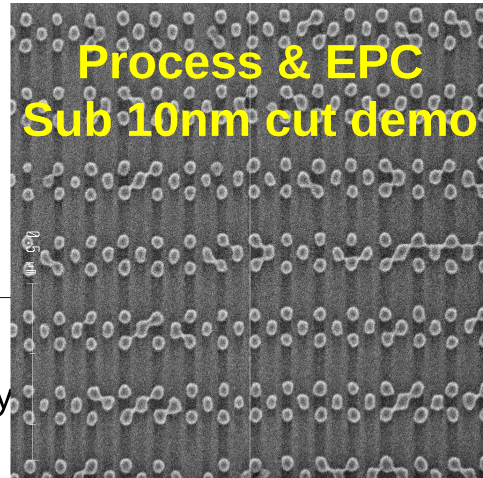
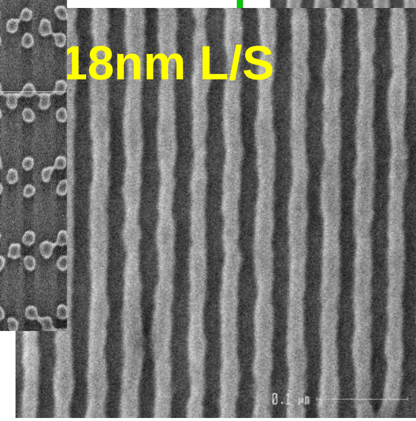
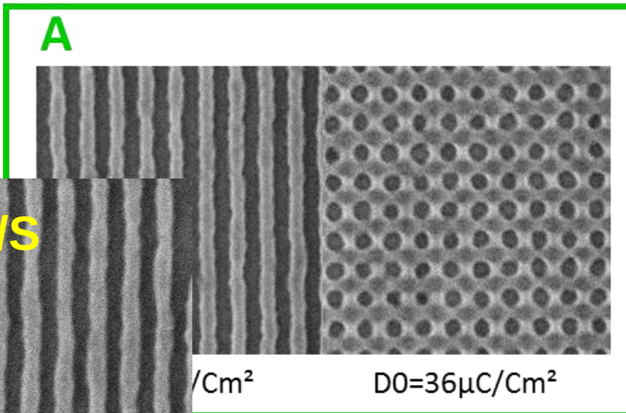
Key results achieved on pre-alpha platform

Tomorrow ?????





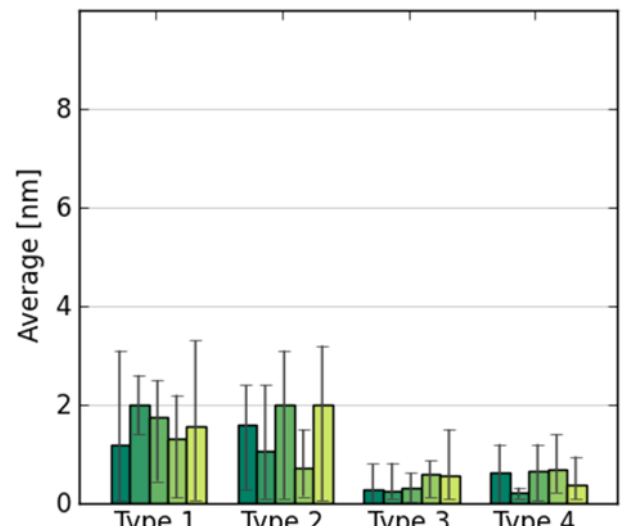


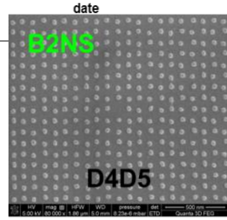


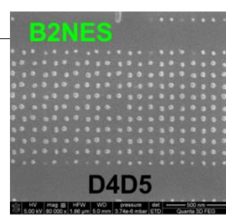
sensitivity on target

Stage stability

Stage prototype







Beam-to-beam control

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Lithography options for tomorrow

- Optical lithography
  - 193nm
  - EUV
- E-Beam direct write lithography
- Self Aligned Ligraphy by block copolymers
- Imprint lithograhy

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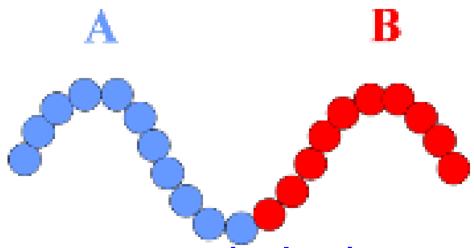
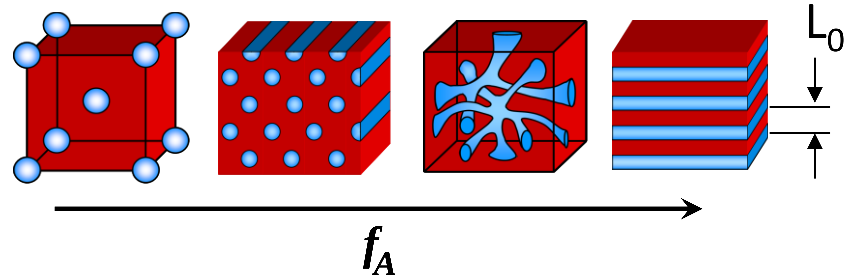
Block copolymers…



Different morphologies accessible
for different compositions

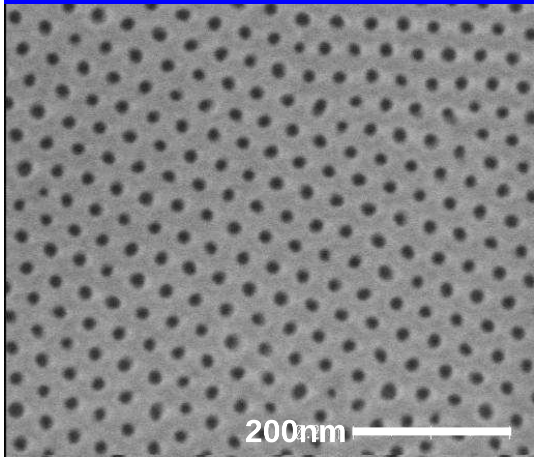


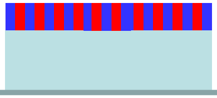
$$f_A = \frac{N_A}{N_A + N_B}$$

Intrinsec period
L_0 < 50 nm

… & Directed Self-Assembly

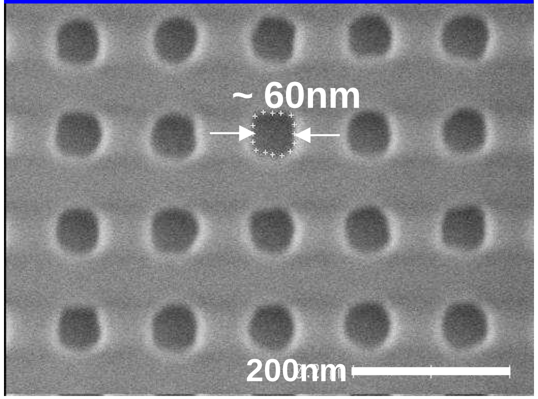
Block copolymer

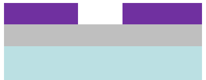




+

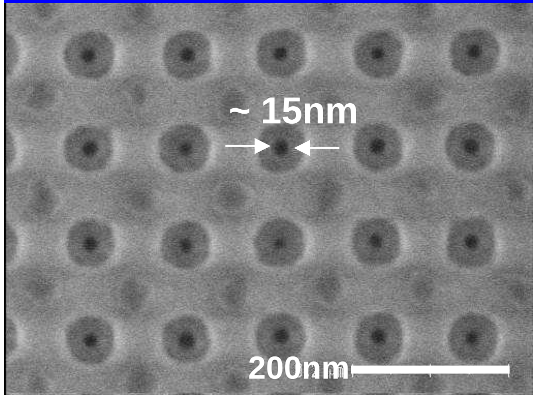
Conventional lithography





=

Directed Self Assembly



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Directed Self Assembly for Microelectronics

Block copolymers self assembly capabilities

- Very high resolution
- Low intrinsic Line Edge Roughness
- Easy process
- Low cost

C-MOS Lithography constraints

- Control the domain orientations (1D - 2D)
- Alignment control with respect to a preview level
- Integration capabilities
- Low defectivity
- Respect of design rules

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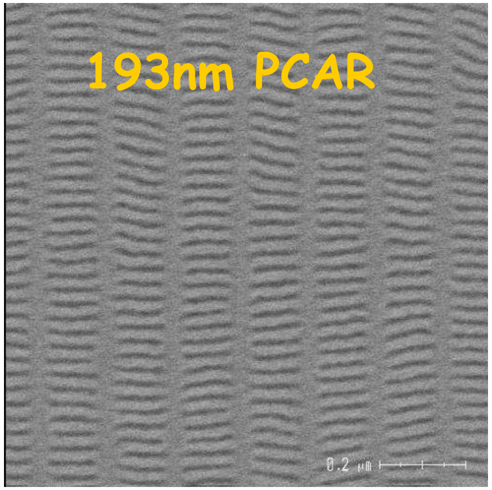
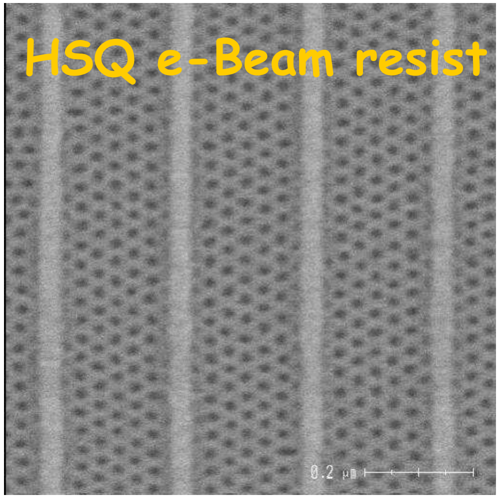
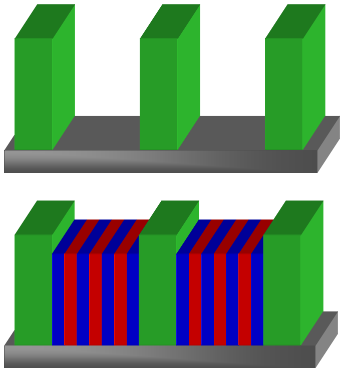
Why grapho-epitaxy preference ?
A versatile process :LETI demonstration

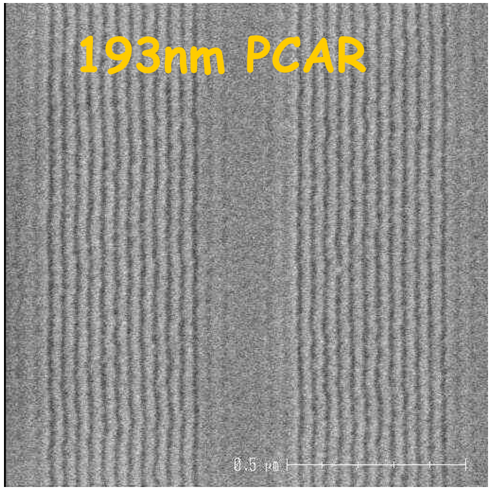


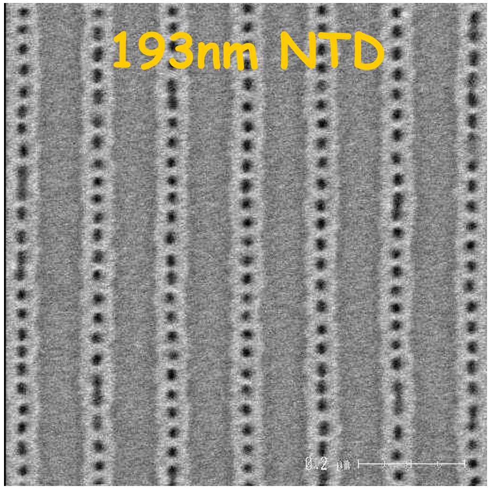


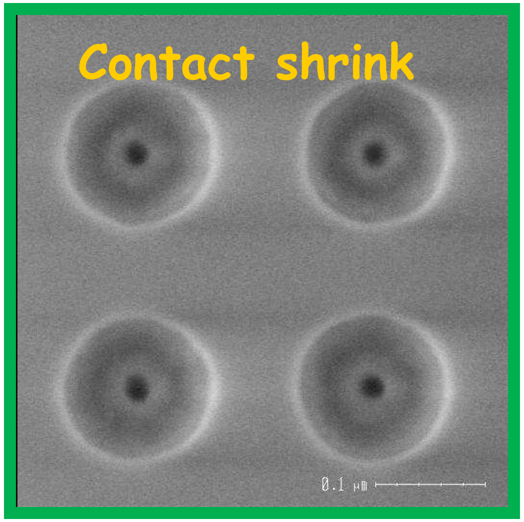
Graphoepitaxy



Leti approach







"Study and optimization of the parameters governing the BCP self-assembly: toward a future integration in lithographic process" X.Chevalier et al,79700Q, SPIE2011

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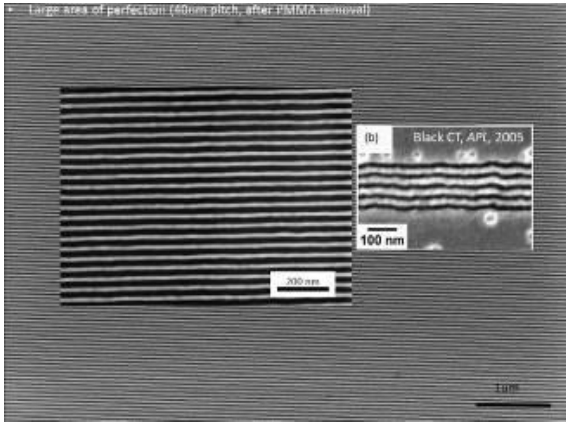
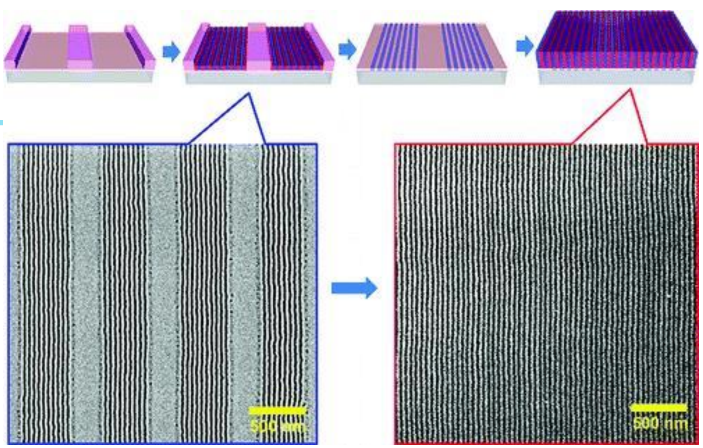
State of the art
Chemical surface modification

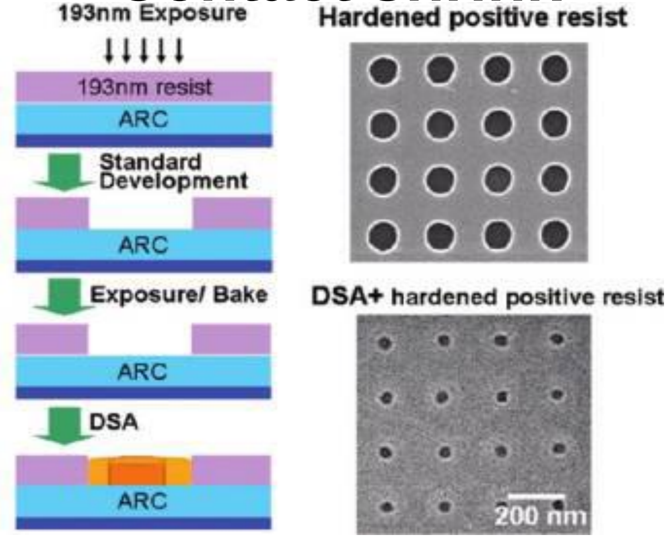


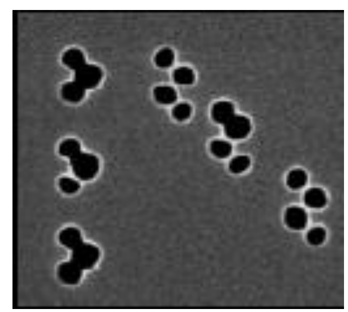
Chi-Chun (Charlie) Liu, Paul Nealey, Sematech DSA workshop, Kobe, Japon 2010

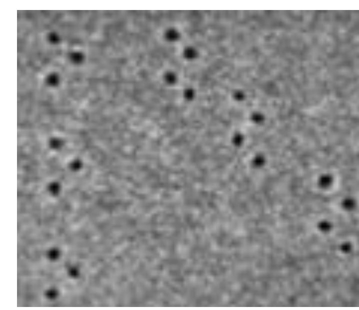


Jeong et al, ACS Nano,VOL. 4, NO. 9, 5181-5186, 2010, KAIST, Republic of Korea

Contact shrink







Cheng et al, ACS Nano,VOL. 4, NO. 8, 4815–4823, 2010, IBM Almaden Research Center

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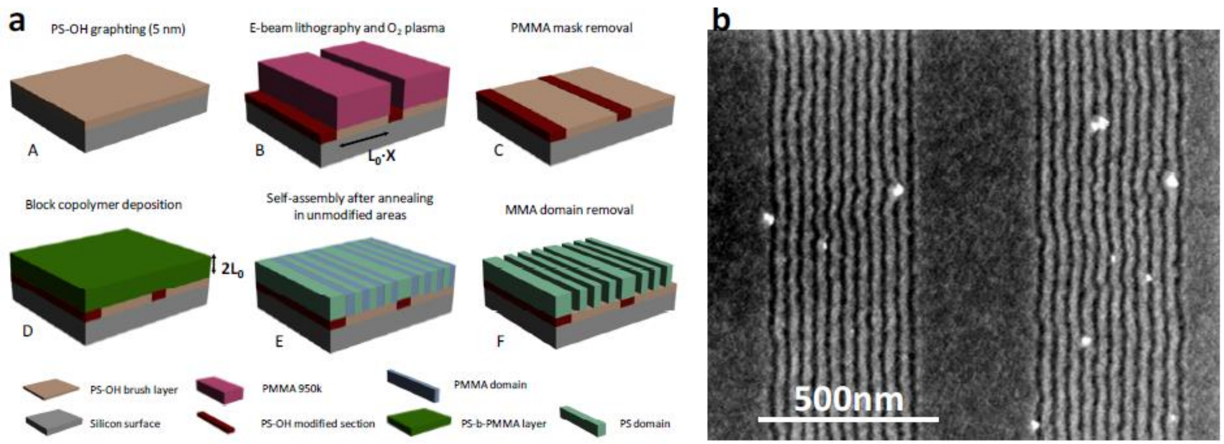
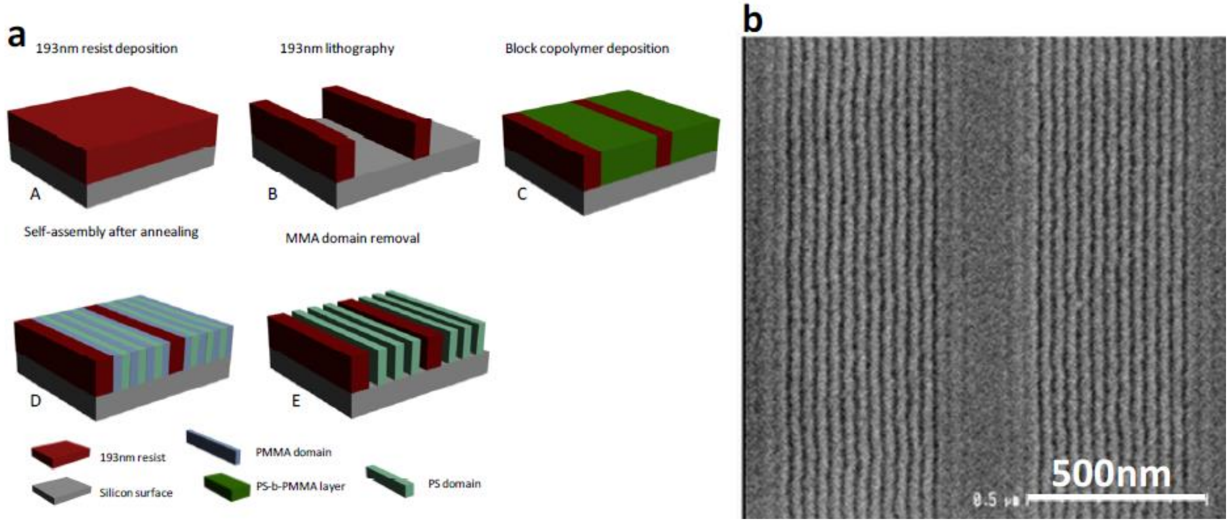
ENIAC LENS program



17,5hp L/S with chemi-epitaxy



15hp L/S with grapho-epitaxy

Proc. SPIE 7970, Alternative Lithographic Technologies III, 79700P (April 01, 2011)

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2nd collaboration initiative launched by CEA-LETI

Insertion of Directed self Assembly Lithography

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missions

- Push material platforms to maturity
  - From lab scale to industry
  - Evaluate advanced copolymer platform
- Develop 300mm patterning solutions
  - Certify material compatibility with clean room standard
  - Screen DSA material performances
  - Verify transfer capabilities
- Scale-up DSA processes to production level
  - Compatibility with design rules
  - Respect of ITRS standard : defectivity, throughput…

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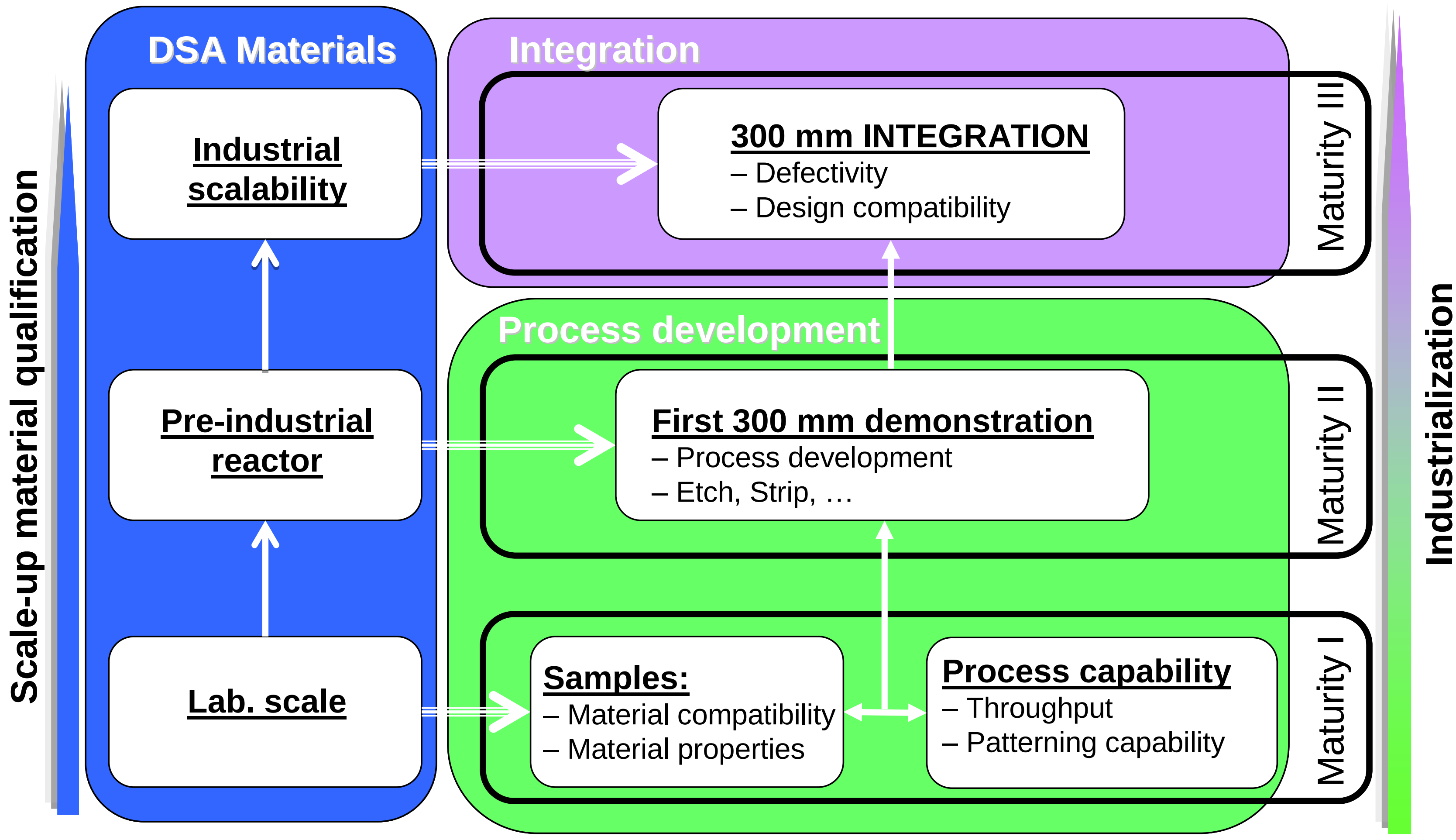
How to go from R&D to industrial ?

A production-oriented consortium



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In few words

- Objectives
  - A collaborative program to develop a full DSA solution
  - Joint work in LETI environment on material, processes, demonstration & integration
  - A cluster open to materials and equipments' suppliers, IDM, EDA

- Partnership status – May 2013
  - DSA material development
    - Copolymer material industrial partener
    - Collaboration with other laboratories & resist partners
  - Equipment suppliers
    - 2 industrial partners
  - End users
    - Bilateral work with

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Key achievement

- Process implementation
- Basic case demonstration : contact shrink application
- Density improvement : contact multiplication
- Modelling

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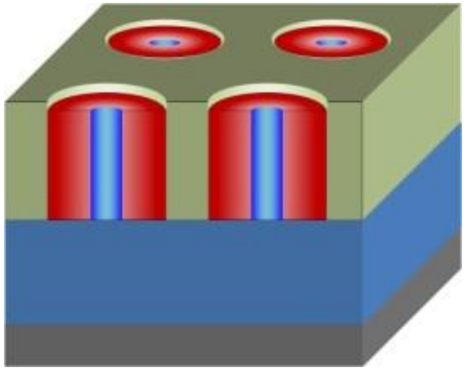
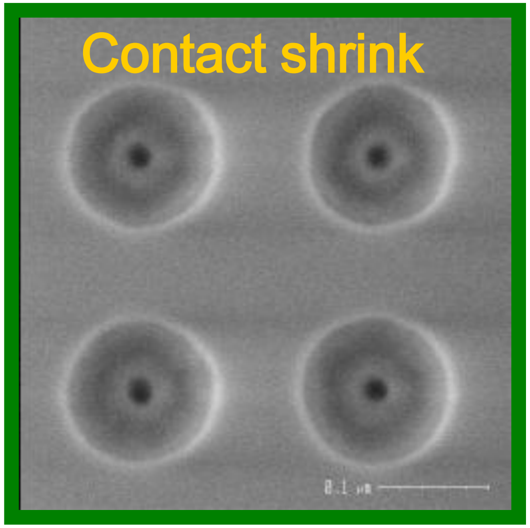
DSA 300 mm process implementation

- ✓ No metallic contamination in polymers
- ✓ POR using a cylindrical polymer PS-*b*-PMMA from Arkema with L_0=38nm
- ✓ Spin casting solvent : PGMEA
- ✓ Brush bake: 230C / 1min
- ✓ Non grafted brush removal : using PGMEA
- ✓ DSA bake: 245C / 1min
- ✓ PMMA removal processes
- ✓ Pattern transfer by etching

"Pattern density multiplication by direct self-assembly of BCP: towards 300mm CMOS requirements" R. Tiron et al, - 8324-23, SPIE2012

BCP self-assembly by graphoepitaxy





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300mm new process capabilities

- 2 advanced 300mm tracks - Q4 2012
  - **SOKUDO DUO** track
    Delivered October 23rd 2012

TEL LITHIUS track
Delivered December, 19th 2012

- To address R&D lithography programs at CEA-Leti
  - Multi-beam through **IMAGINE** project
  - DSA projects via **IDEAL** program
- JDP programs signed
  - Privileged partnerships – Bilateral activities

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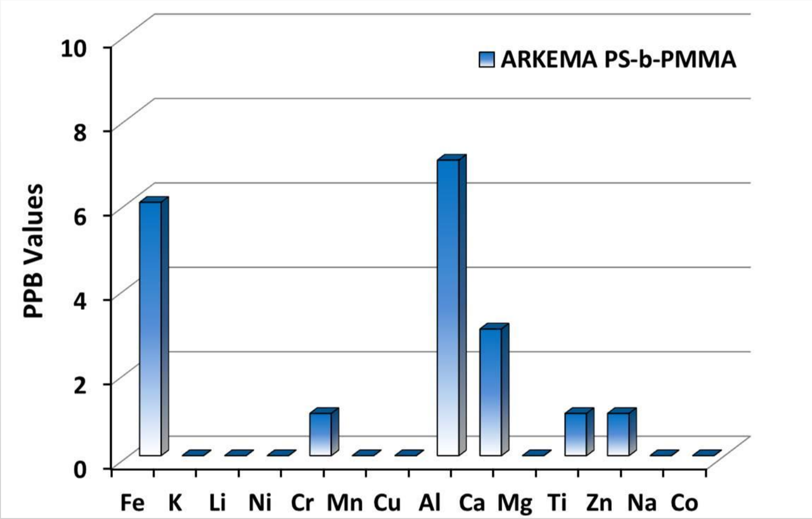
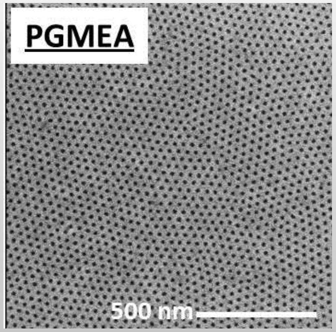
Polymer compatibility with CMOS requirements

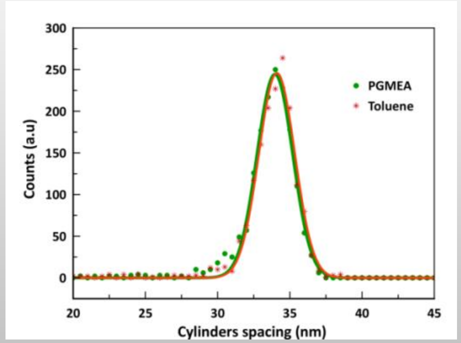
Polymers metallic contamination



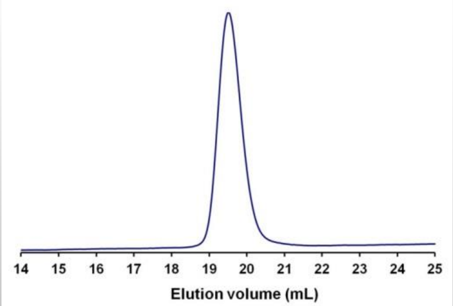
Metallic contamination < 10 ppb

Track-compatible solvents





Polymers arhitecture



chains dispersity < 1,1

Polymers solution fully compatible with current lithographic CMOS requirements

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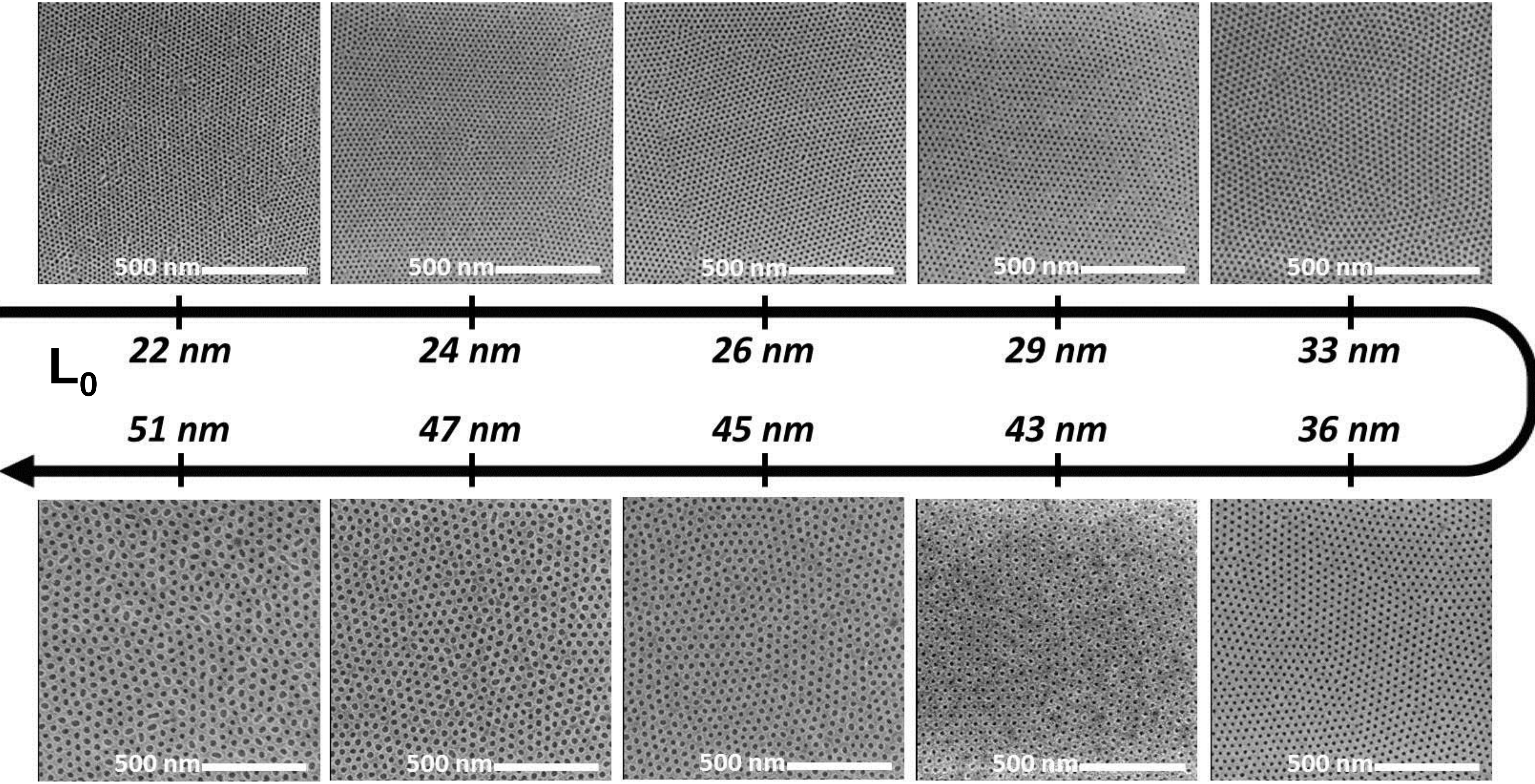
PS-*b*-PMMA tunability vs. node extendibility



X.Chevalier et al, Proc of SPIE 2013, 8681-5

Feature-size under chemical control (molecular weight, composition...) L_0 : 20 to > 50nm demonstrated

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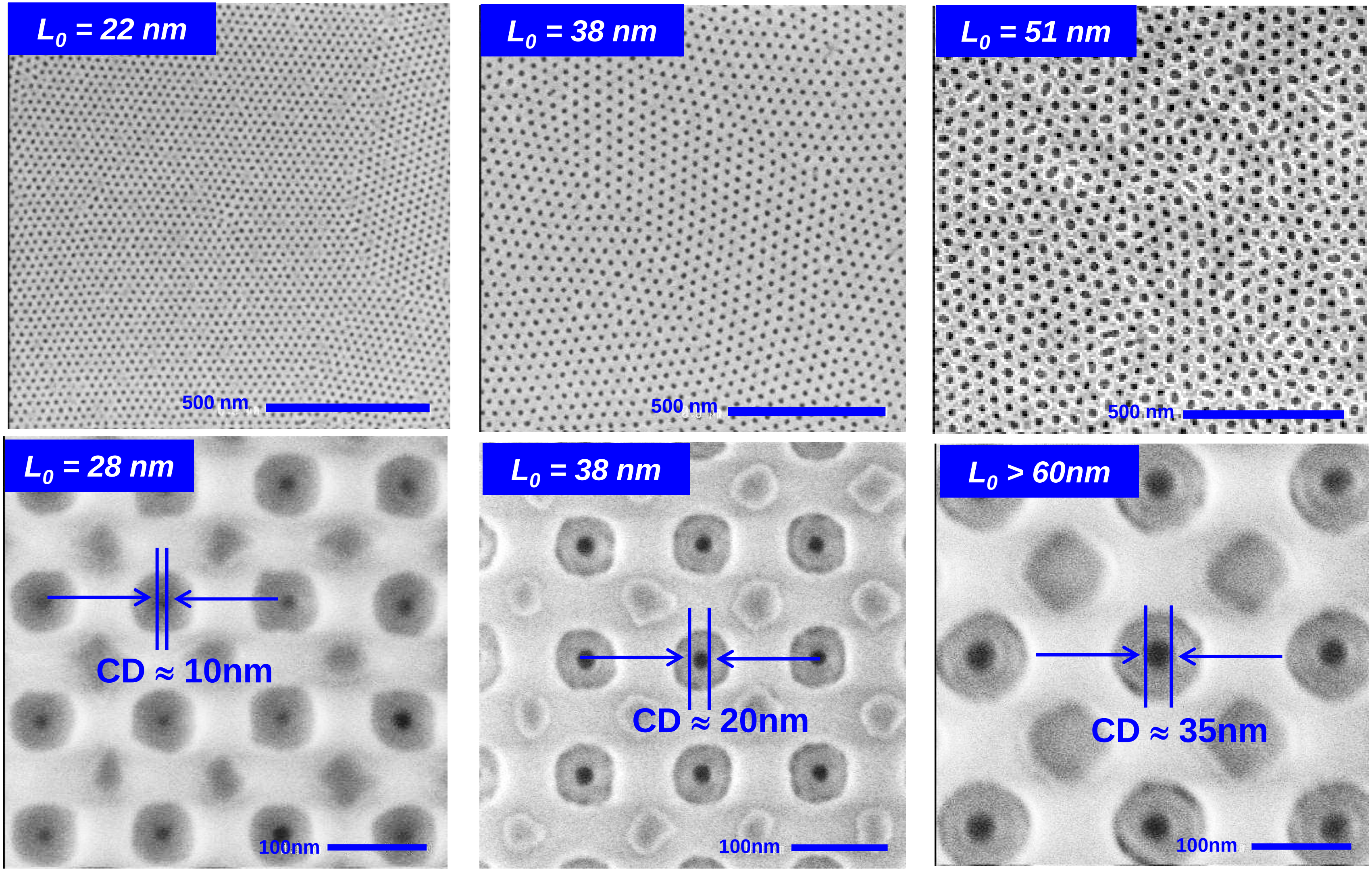
Broad range of PS-*b*-PMMA

X.Chevalier et al, SPIE Paper 8680-5



Customizable PS-*b*-PMMA polymers with various pitch demonstrated

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Key achievement

- Process implementation
- Basic case demonstration : contact shrink application
- Density improvement : contact multiplication
- Modelling

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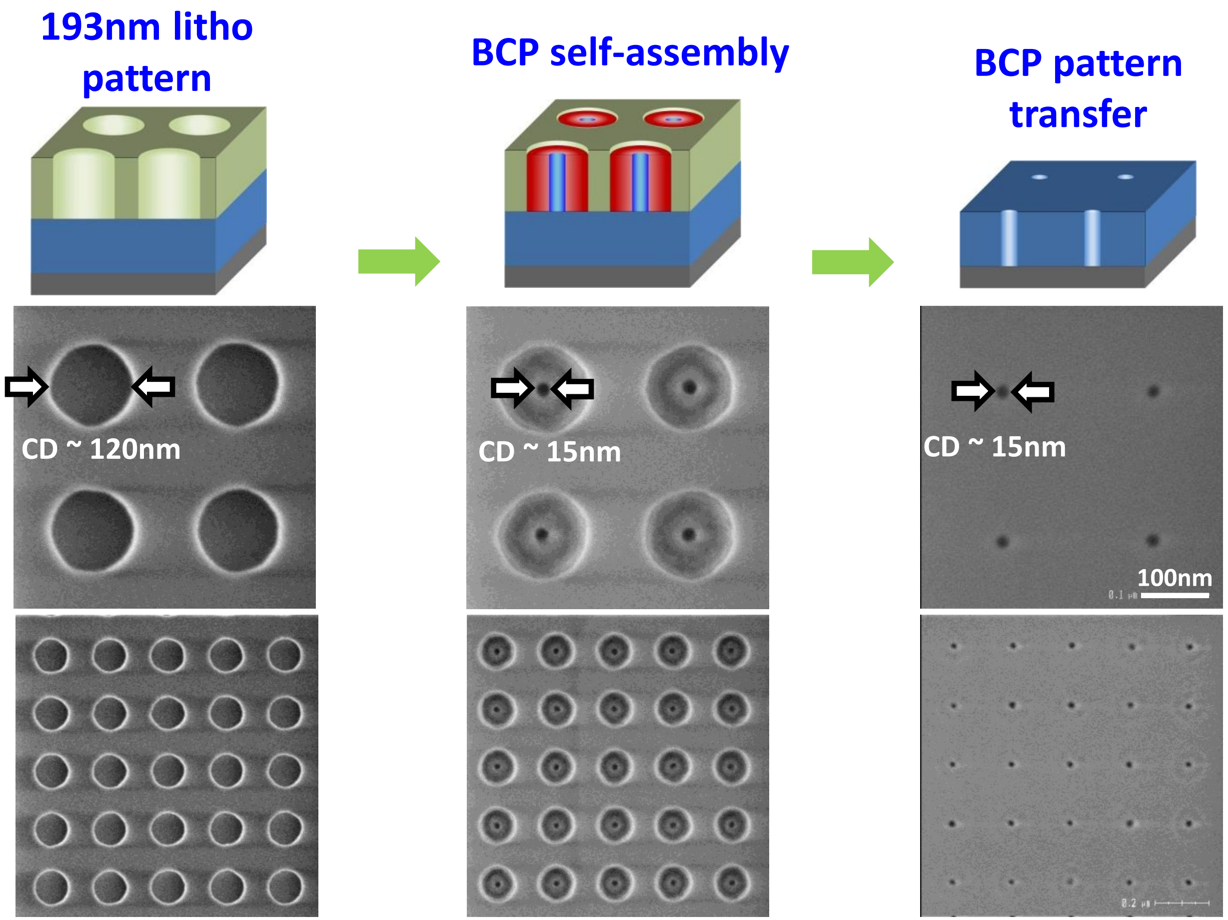
DSA LETI's 300 mm pilot line



DSA Process of reference (lithographie and etch) available on 300 mm pilot line in Leti

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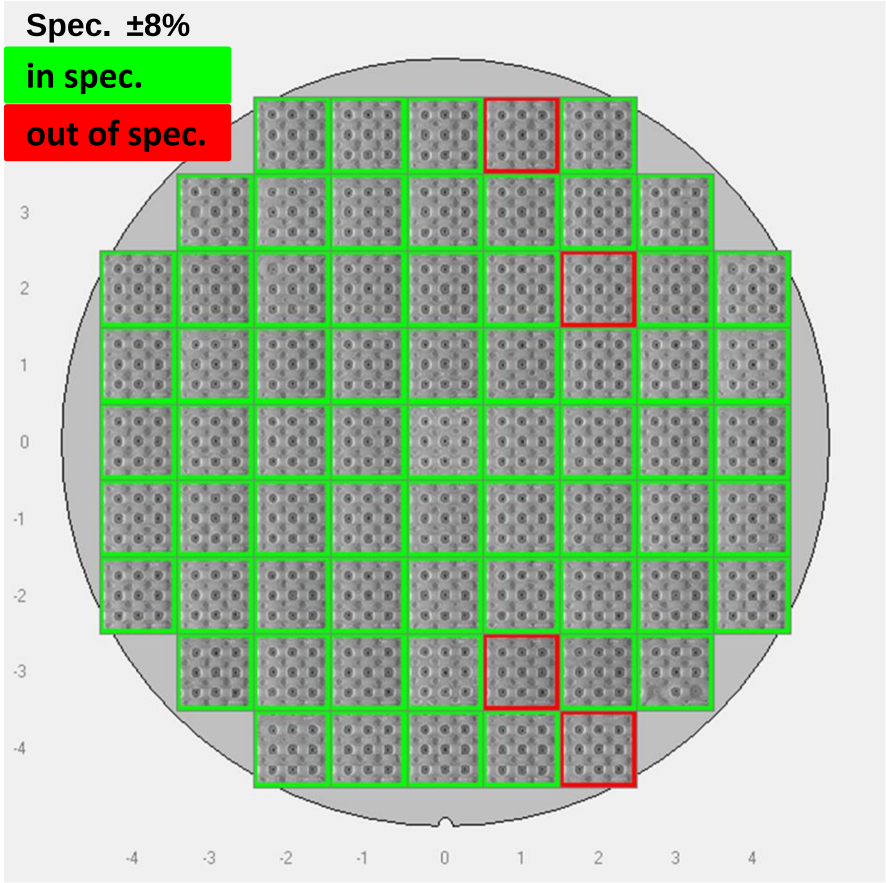
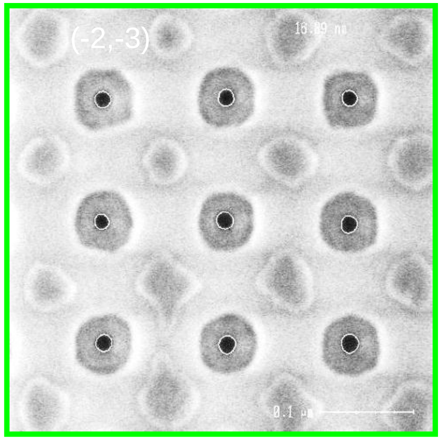
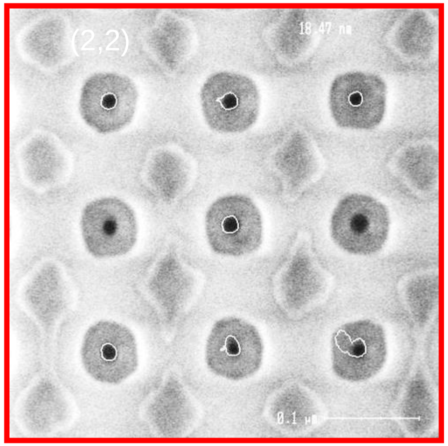
CD uniformity after BCP self-assembly

E-beam litho







Guiding patterns (e-Beam litho.) CD_{guide} = 56.3nm / 3σ = 1.2nm
After BCP self-assembly CD_{BCP} = 17.0nm / 3σ = 2.2nm
Metrology @ theses dimensions need to be improved

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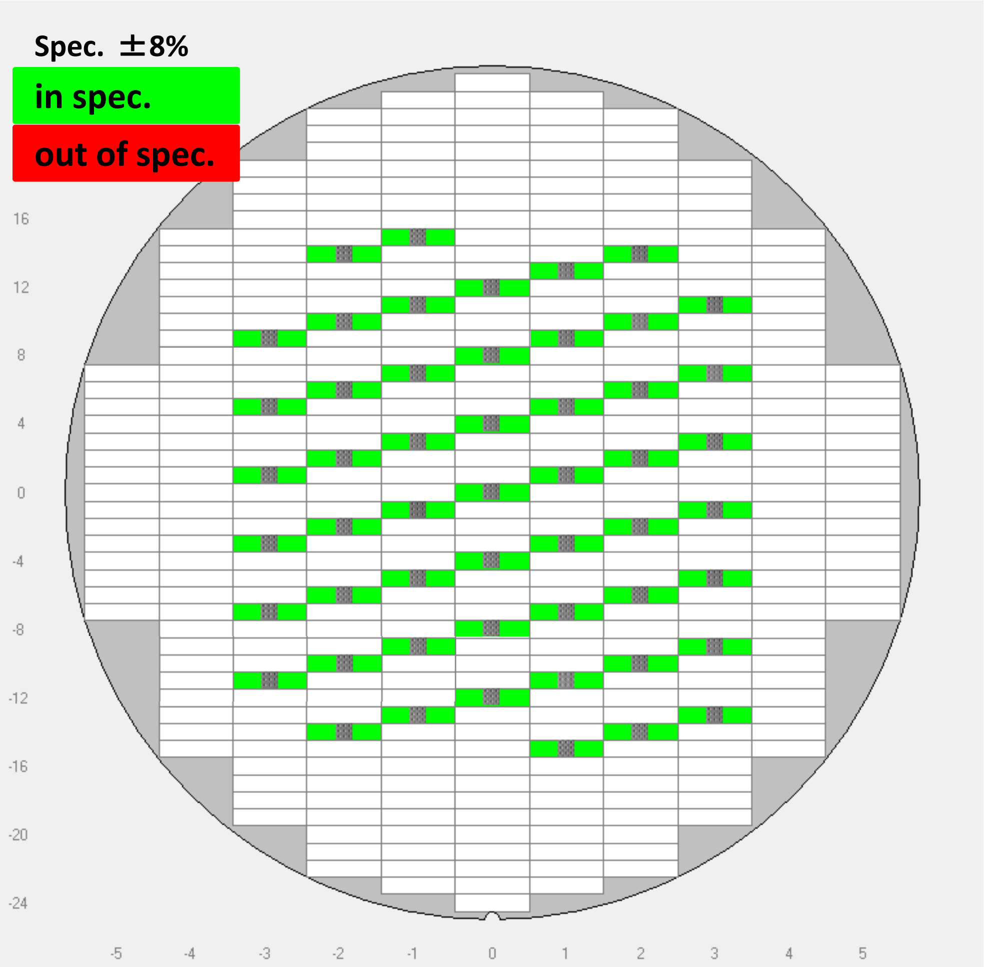
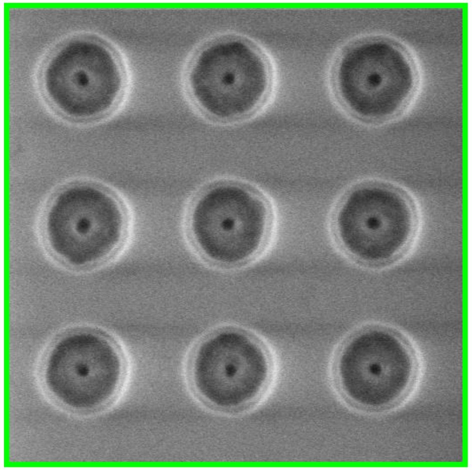
CD uniformity after BCP self-assembly



193nm dry litho



Guiding patterns (193nm litho.)
After BCP self-assembly

CD_{guide} = 116.5nm; 3σ = 2.7nm
CD_{mean} = 21.6nm; 3σ = 1.7nm

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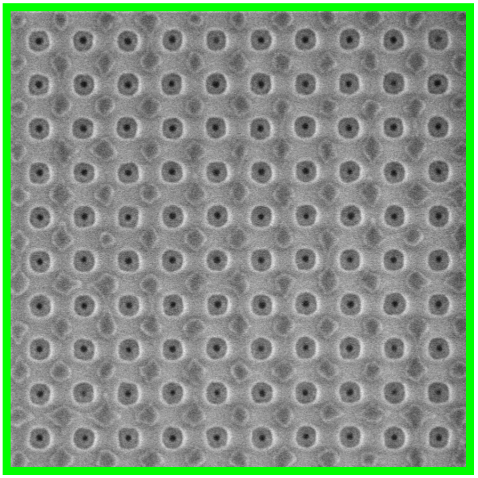
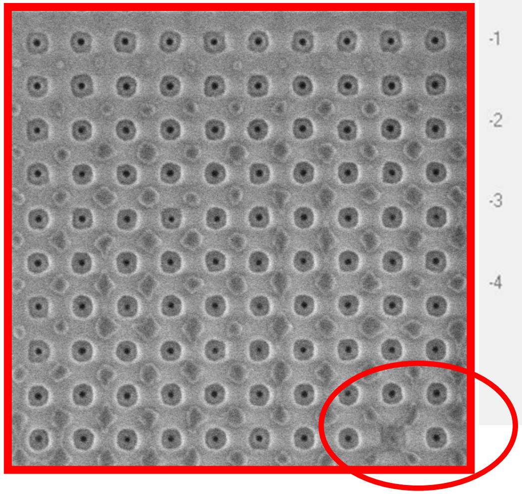
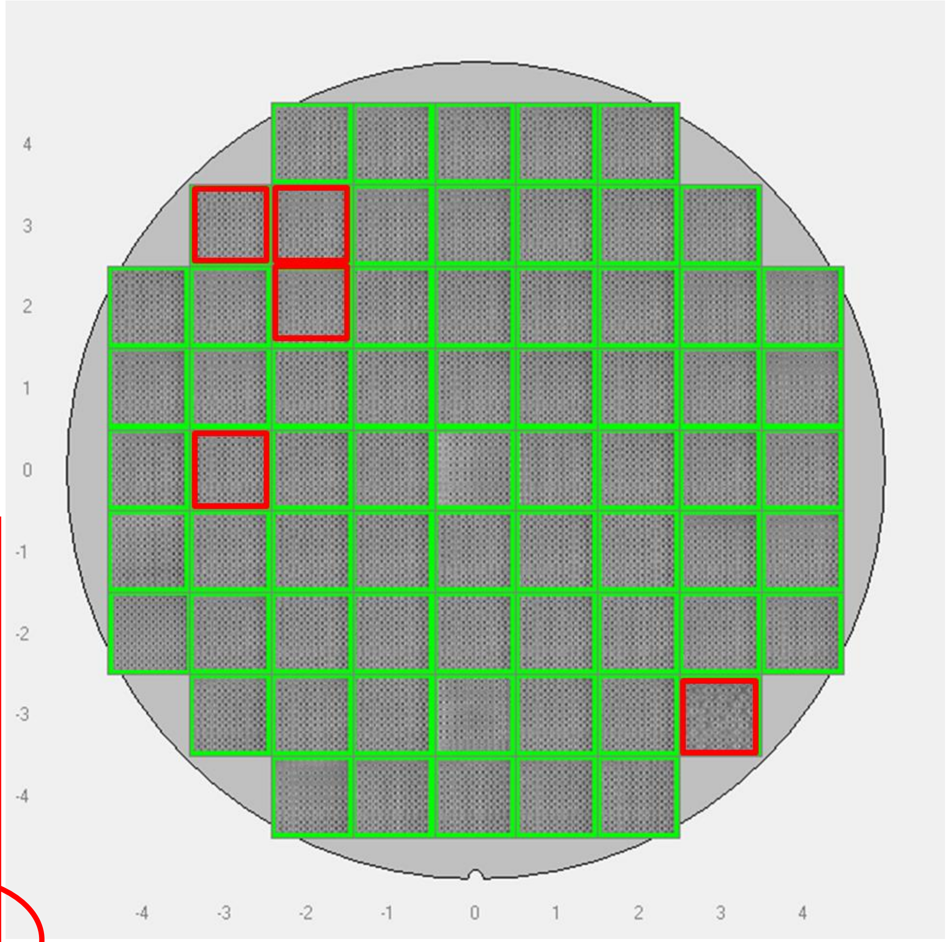
CH shrink: defectivity evaluation vs. process

- 300 mm process, manual spin coat
- Guiding patterns : e-Beam litho + etch
- CD SEM-images @ 100K
- 68 chips / 100 contacts per chip
- 6800 meas. points / 5 missing contacts
- **99,93 %** valid contacts







Defect from guiding patterns

Best process: 99.93 % of good contacts on the wafer

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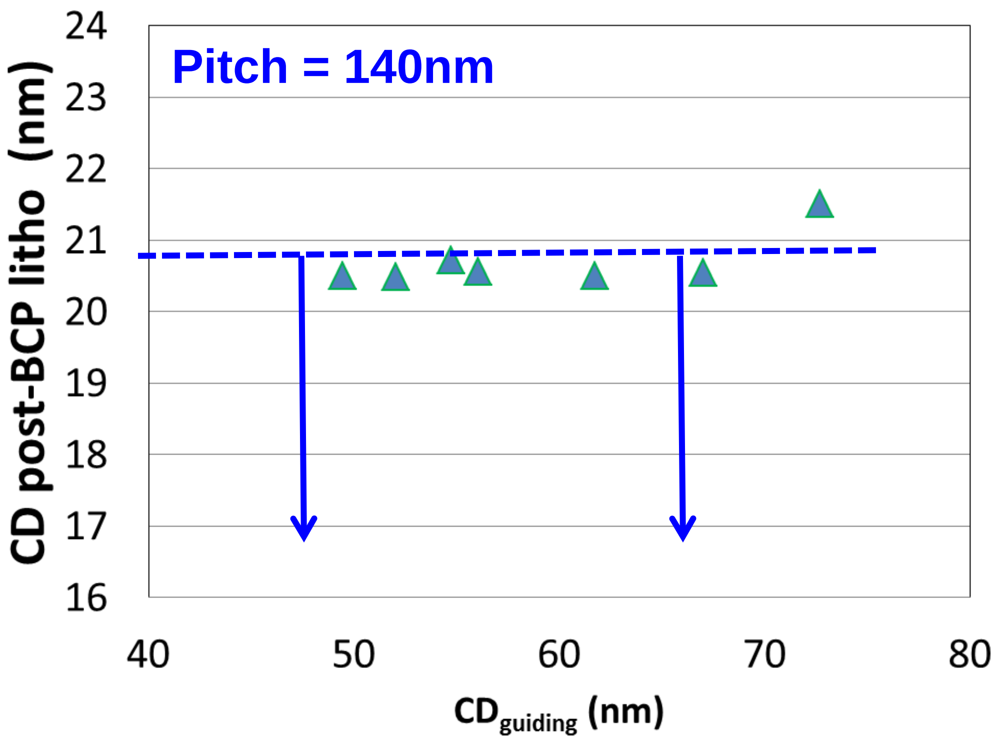
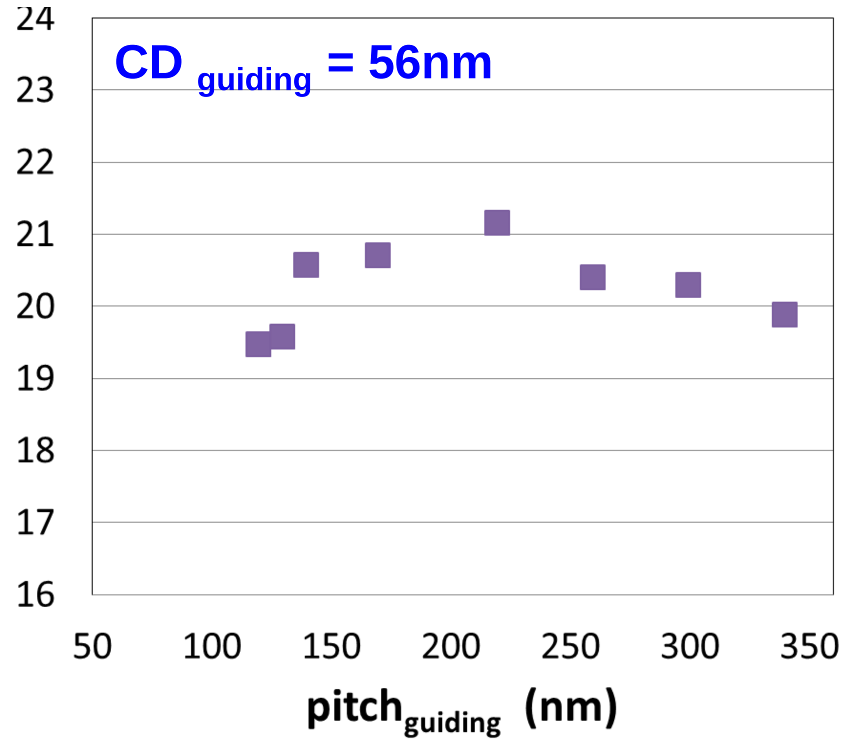
CD_{BCP} vs. CD_{guide} and $pitch_{guide}$

E-beam litho





BCP adsorbs ±10nm of CD dispersity

Slow CD_{BCP} variation with the pitch

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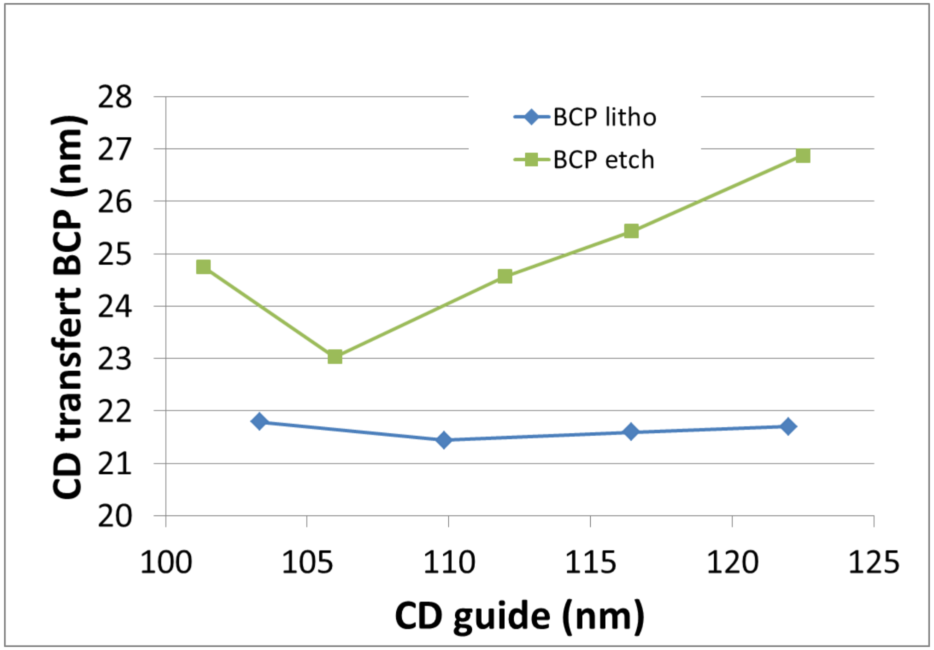
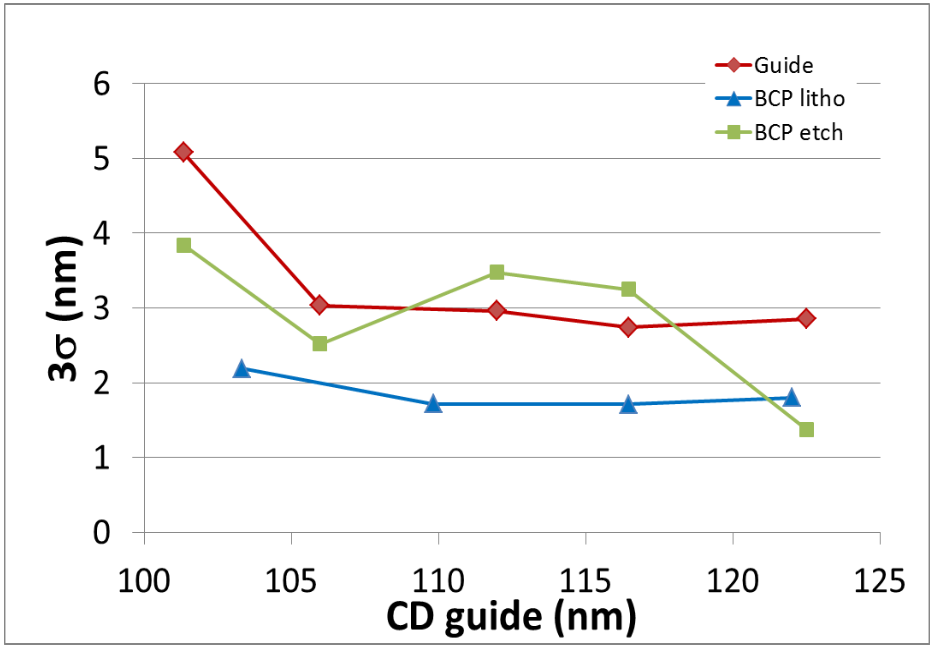
CD of BCP monitored after litho & etching

193nm dry litho





Good CD control after BCP litho. (CD dispersity is improved)
Etching step need to be optimized *(here PMMA removal only by wet)*

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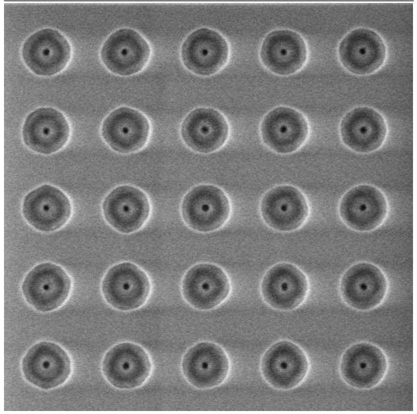
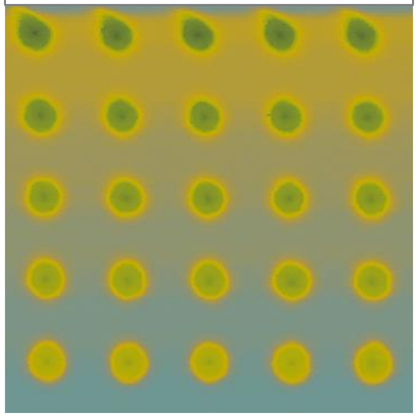
Contact hole characterization

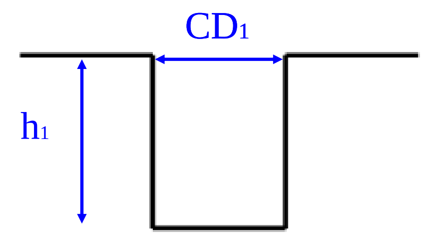
CD SEM

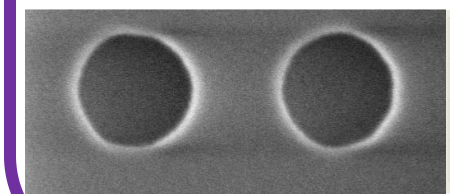


AFM-3D

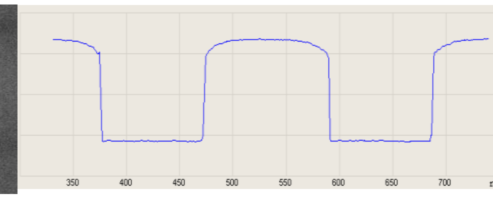


Guiding patterns



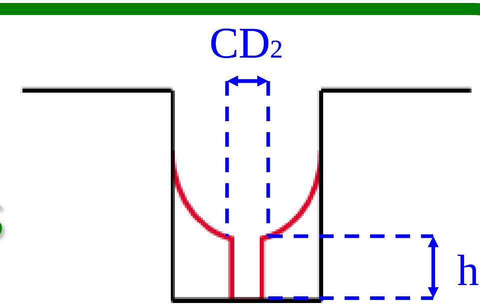


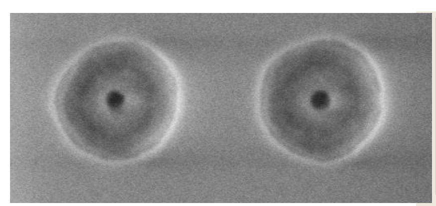
CD-SEM



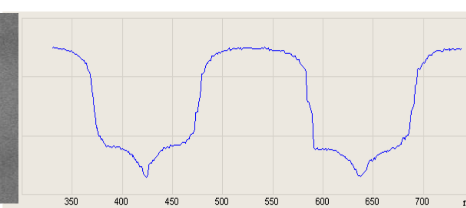
AFM

BCP patterns





CD-SEM



AFM

- CD_1 and CD_2 by CD-SEM
- h_1 and h_2 by AFM-3D

Need to combine different metrology tools to fully characterize patterns (hybrid metrology)

J. Foucher et al, Proc of SPIE 2013, 8681-5

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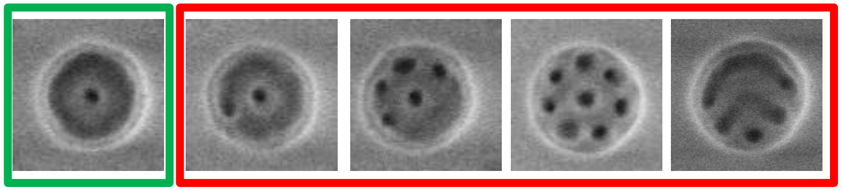
CH shrink: defectivity evaluation vs. process 1/2

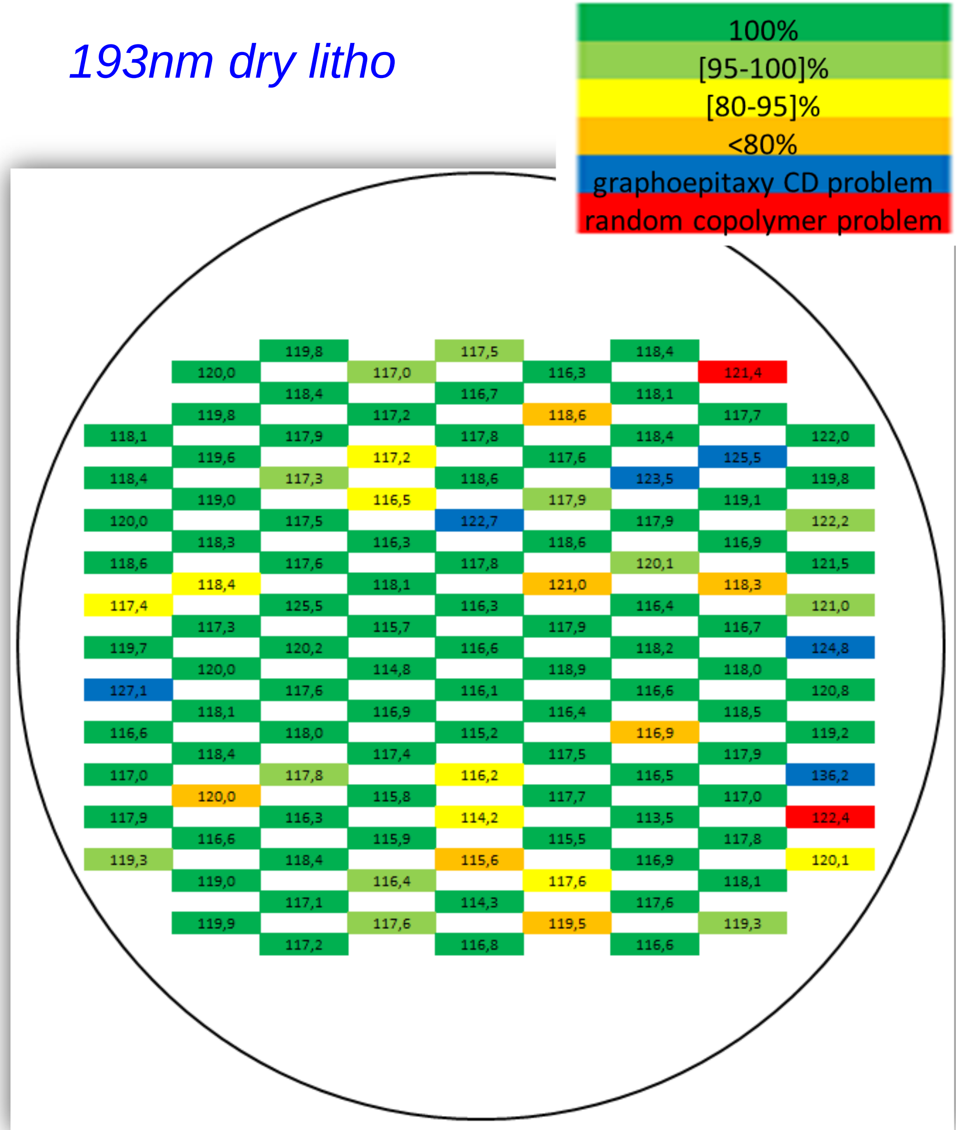
Good contact **Defects**



- 300 mm POR
- manual spin coat
- CD SEM-images @ 120K
- 130 chips / 3250 meas. point
- > 70% of chips with zero defects
- **95,15 %** valid contacts

This methodology allow us to benchmark processes and materials

193nm dry litho



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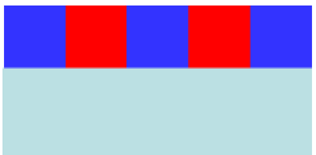
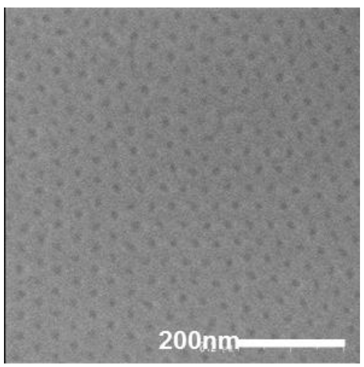
PMMA removal: wet treatment

CD-SEM

AFM

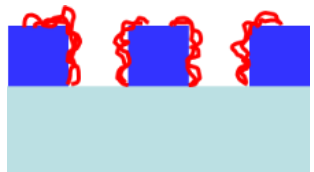
Wo dev

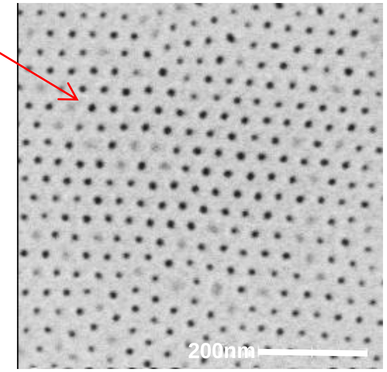


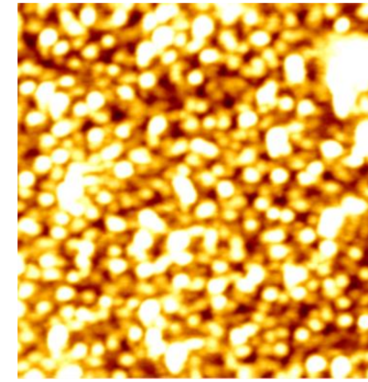


wet dev.

Missing contacts

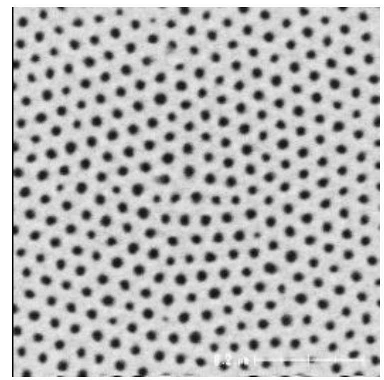


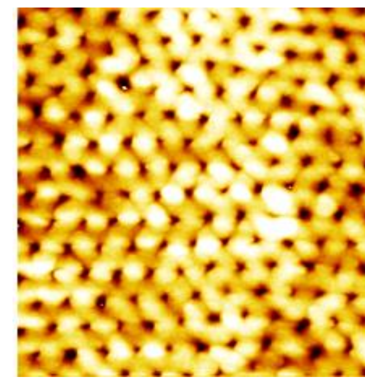




hν + wet dev.

Wet by acetic acid





- Only wet : missing contacts
- Need to depolymerize PMMA before wetting by different exposure treatments (ebeam, 193nm, implantation, etc)

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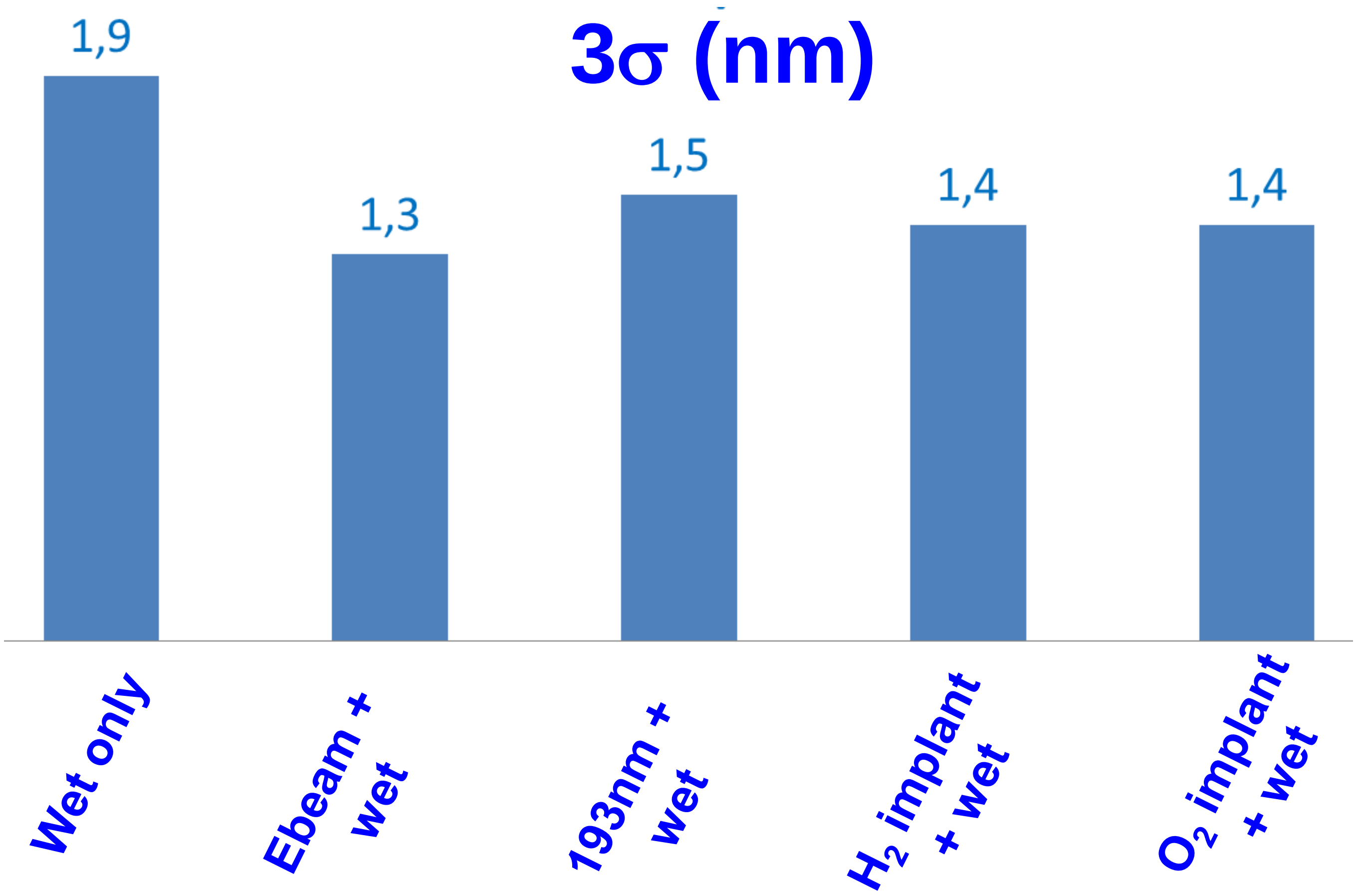
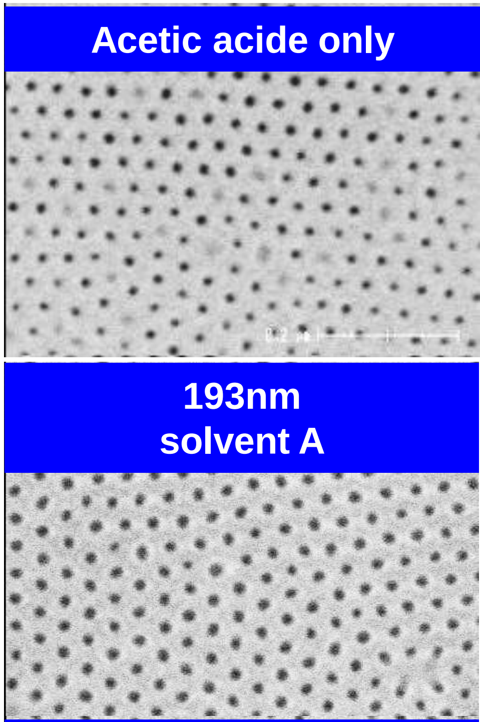
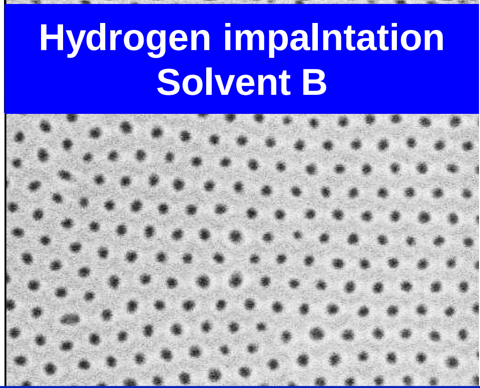
CD dispersity after dif. treatment







- PMMA depolymeriziation before wet improves dispersity
- Acetic acid and different organic solvents 300mm track compatibles are available

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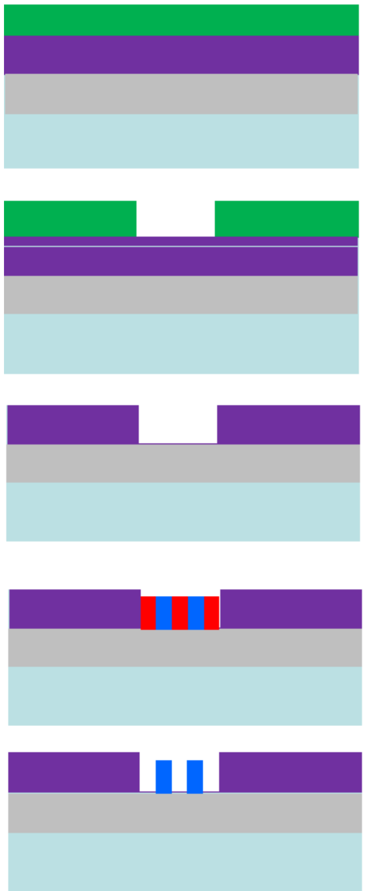
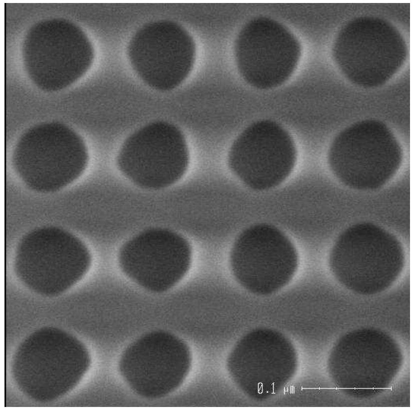
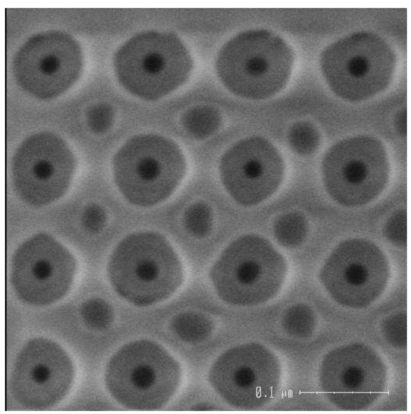
Two integration schemes

1.Double hard-mask

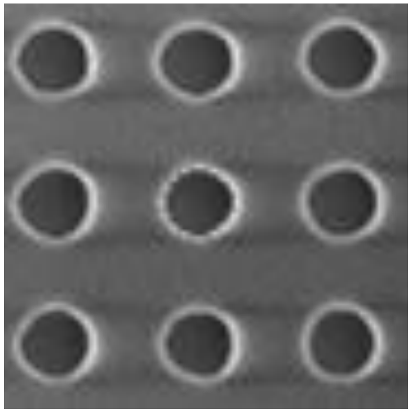
193nm or e-beam

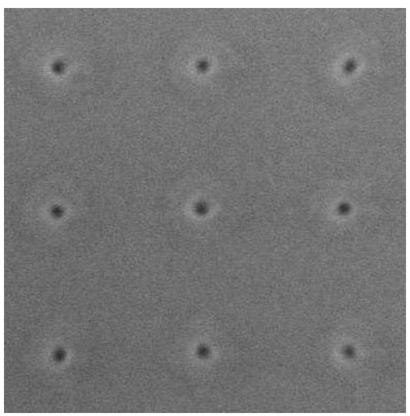


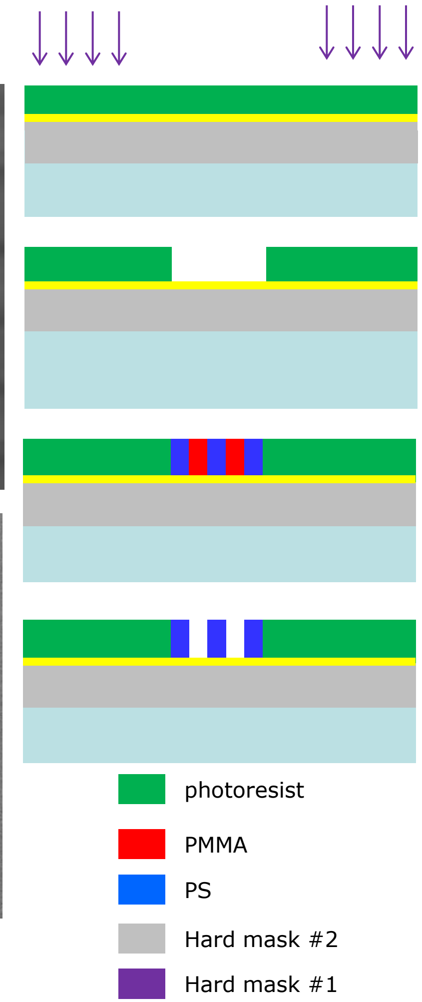




2. NTD Resist







Guiding patterns

DSA patterns

NTD resist approach: less process steps but resist reflow and control of CD during DSA bake still difficult

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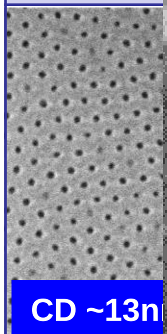
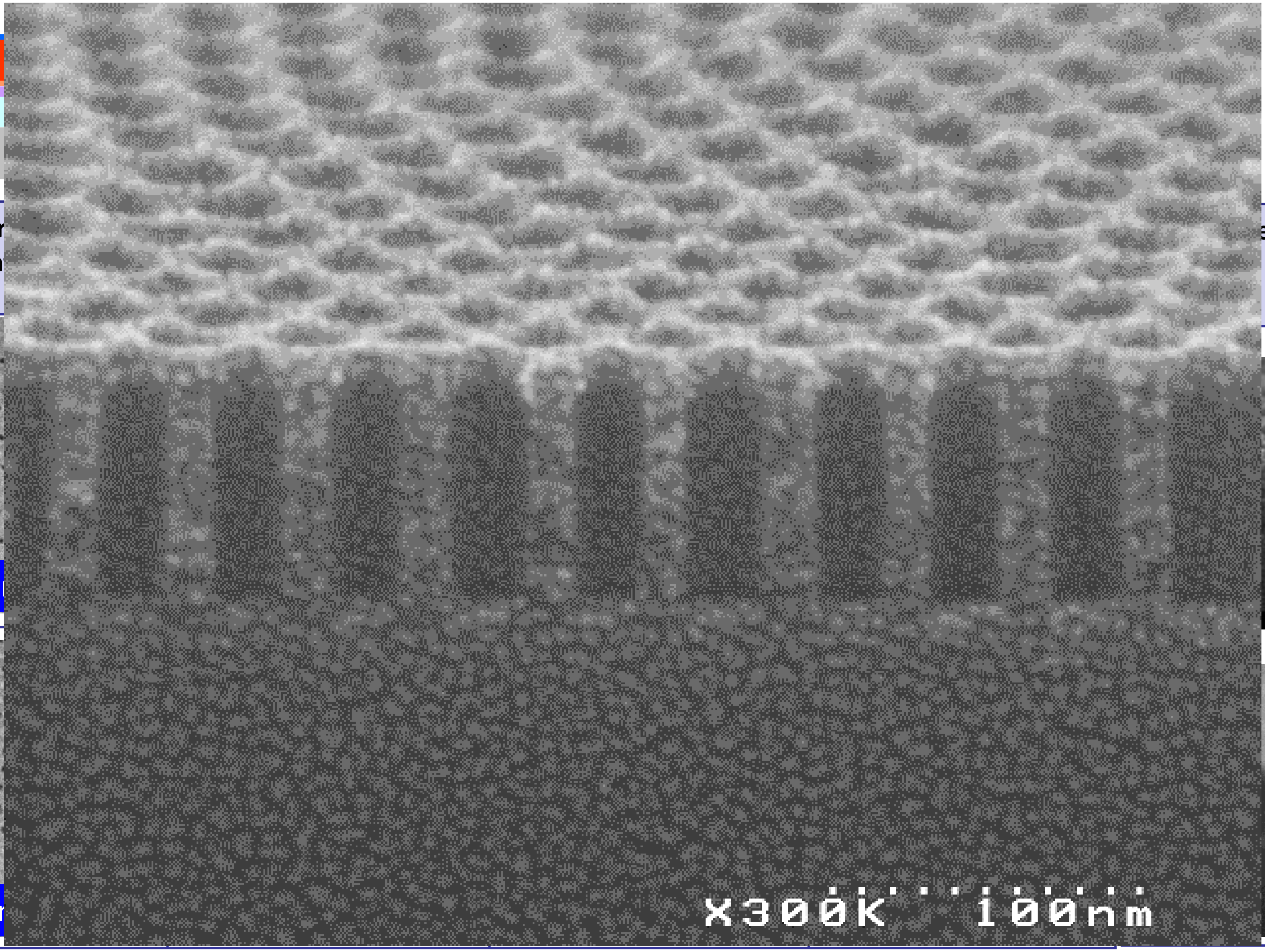
BCP etching optimization

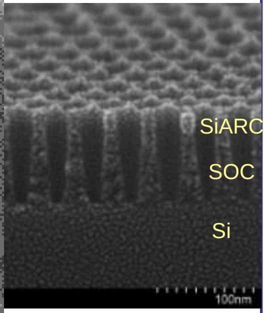
DSA after
trea

er SOC etching

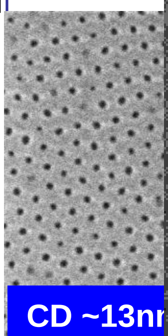
PROCESS 1

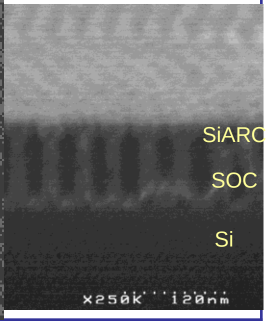






PROCESS 2





PS-PMMA transfer in typical 193 hard-mask is demonstrated

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Key achievement

- Process implementation
- Basic case demonstration : contact shrink application
- Density improvement : contact multiplication
- Modelling

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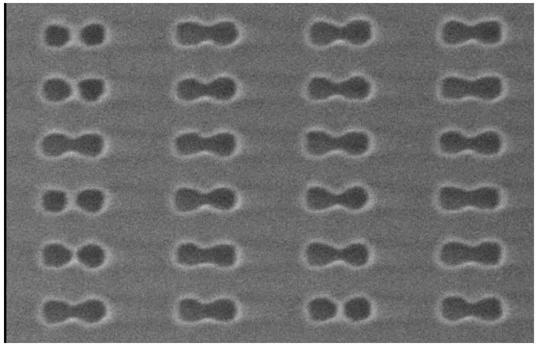
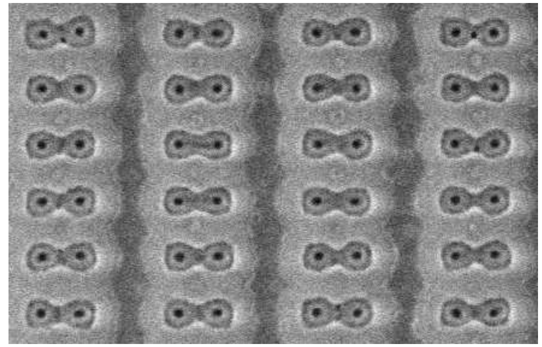
Contact doubling

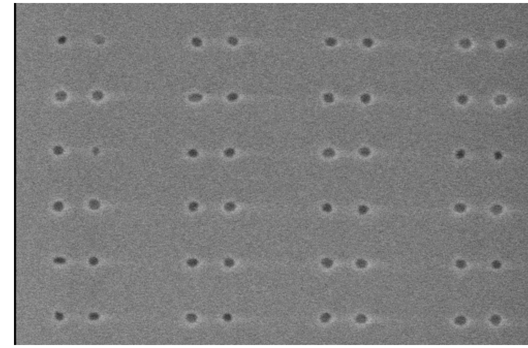
Guiding template 



BCP DSA 

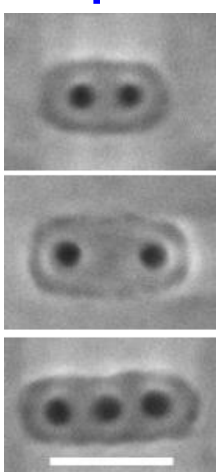


BCP etching 

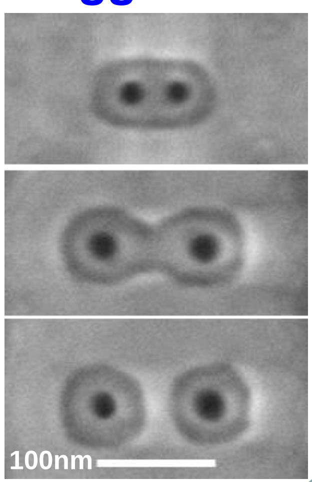


Cylindrical BCP (L0= 38nm) in guiding templates

elliptical



"eggs box"



- Contact doubling demonstrated with DSA
- Pitch sizing possible with contact doubling approach

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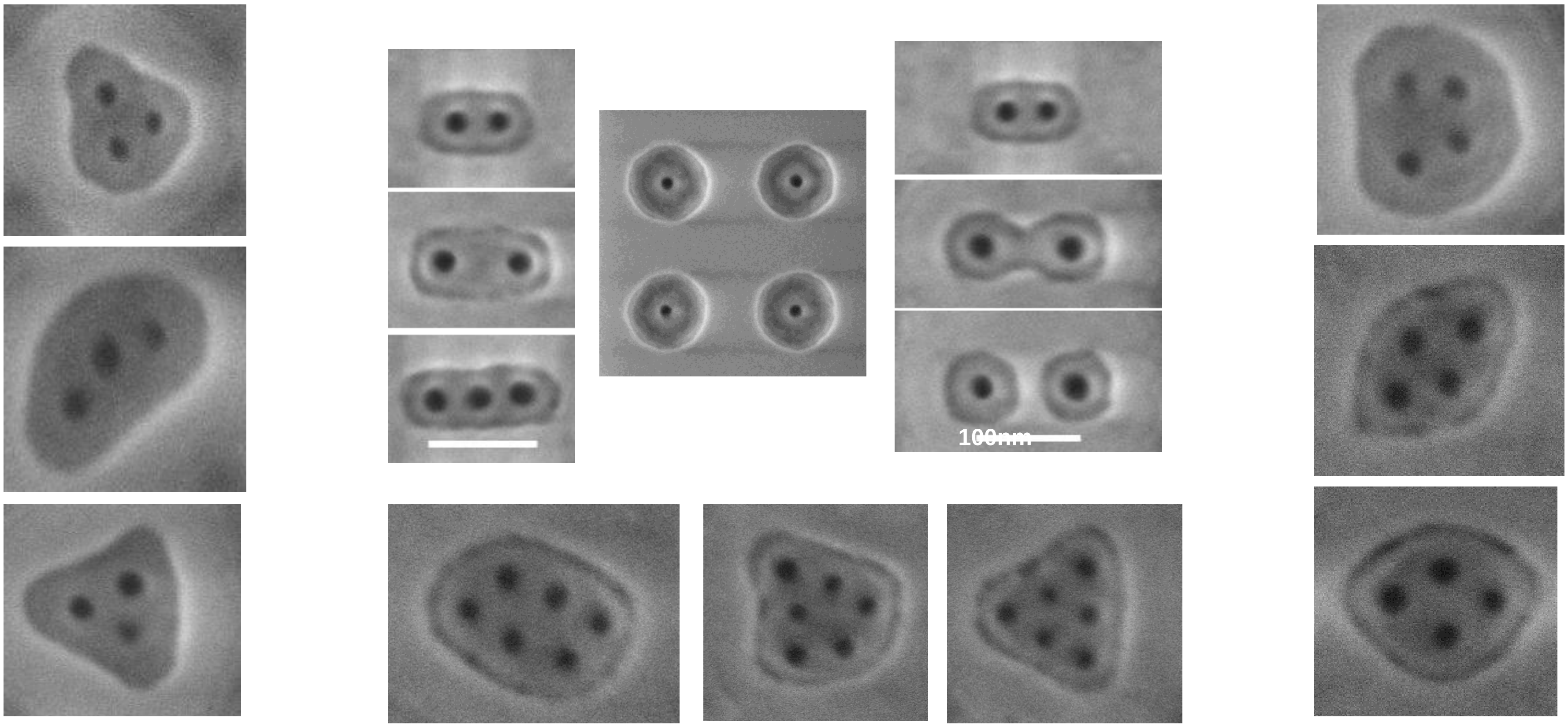
What’s next: Exotic configurations



Complex structures available for contact multiplication by DSA to address design rules (hexagonal symmetry may be broken)

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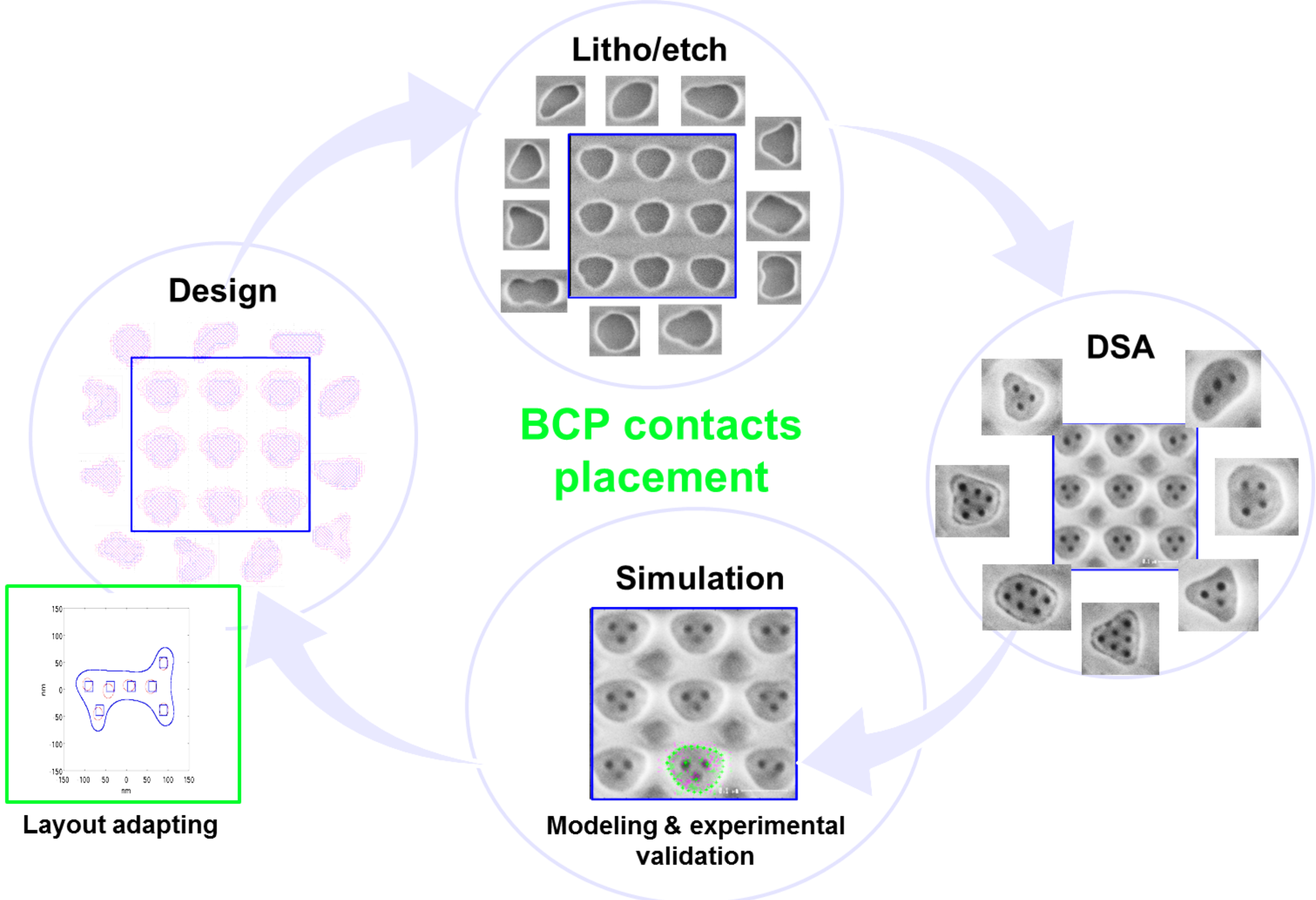
Pattern prediction and simulation



Complex structures available for contact multiplication by DSA to address design rules

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Key achievement

- Process implementation
- Basic case demonstration : contact shrink application
- Density improvement : contact multiplication
- Modelling

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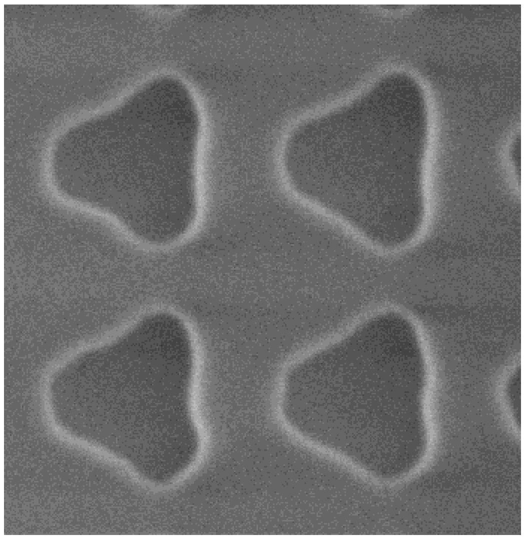
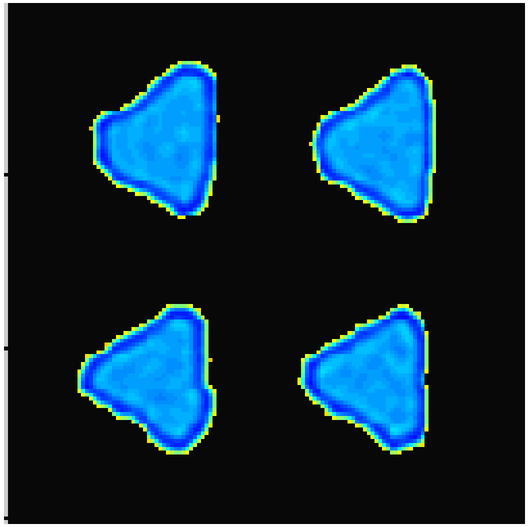
DSA physical modeling

Model based on spinodal decomposition and the Cahn-Hilliard equation

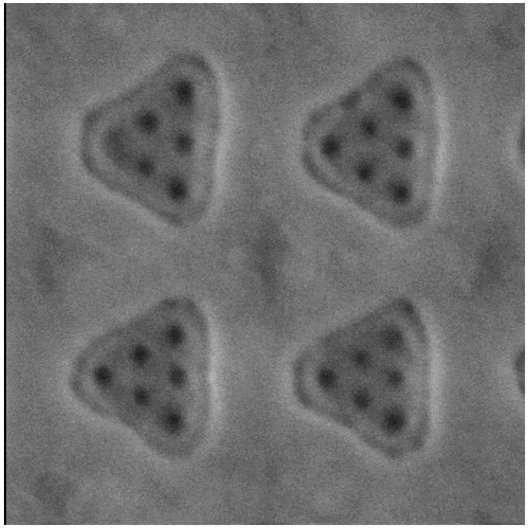
Guidings



Simulation



Experimental



Physical modeling will be used to calibrate a compact model

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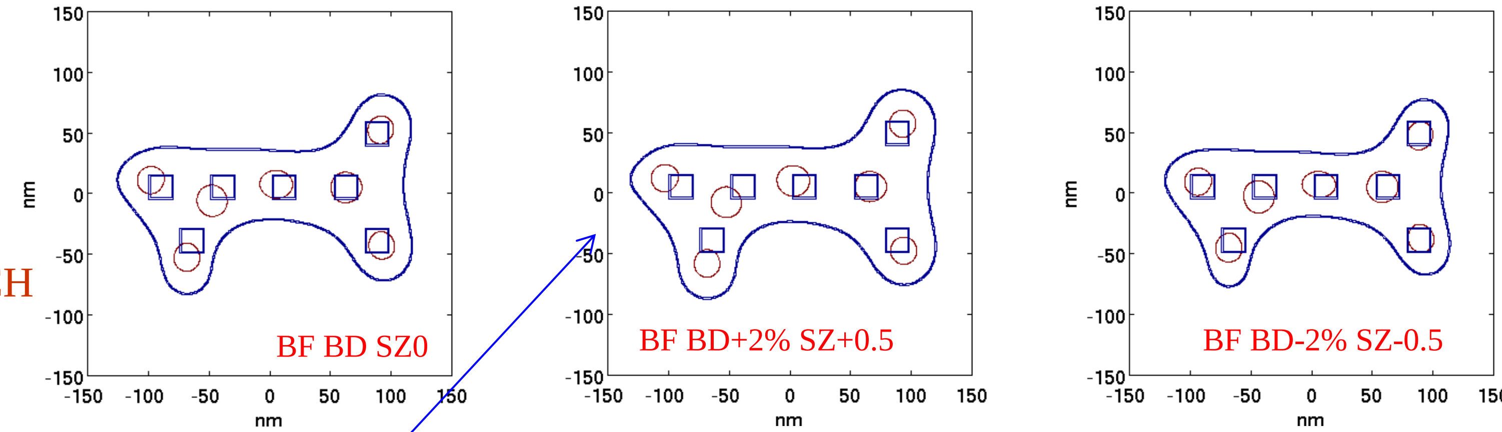
Predicting polymer structures: compact model

□ Design

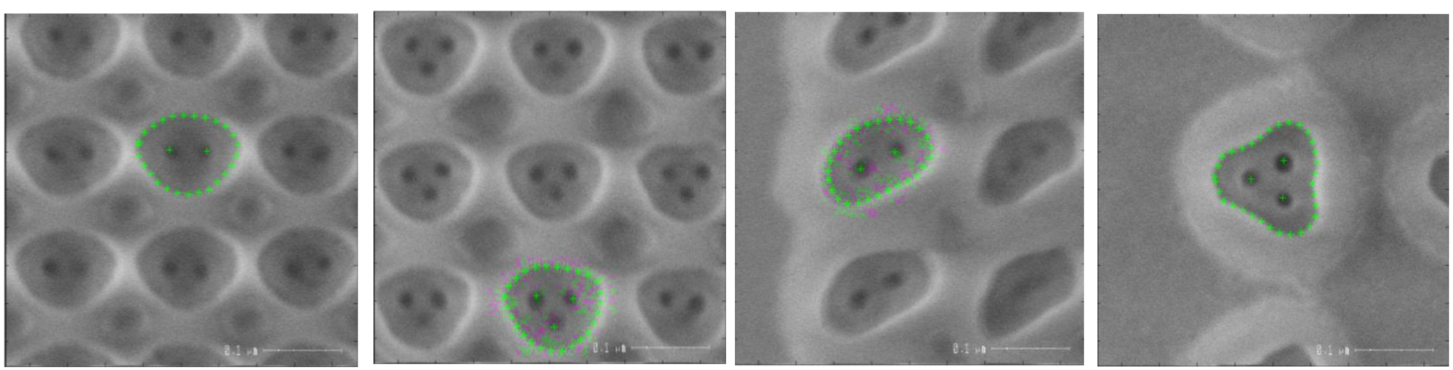
○ Calculated CH placement



Simulation contour

Contour variation w.r.t. dose, focus and mask CD error variations

Experimental validation



Extracted Contour

Calculated CH position

CH position on wafer

Pattern multiplication: process available and simulation tools under development

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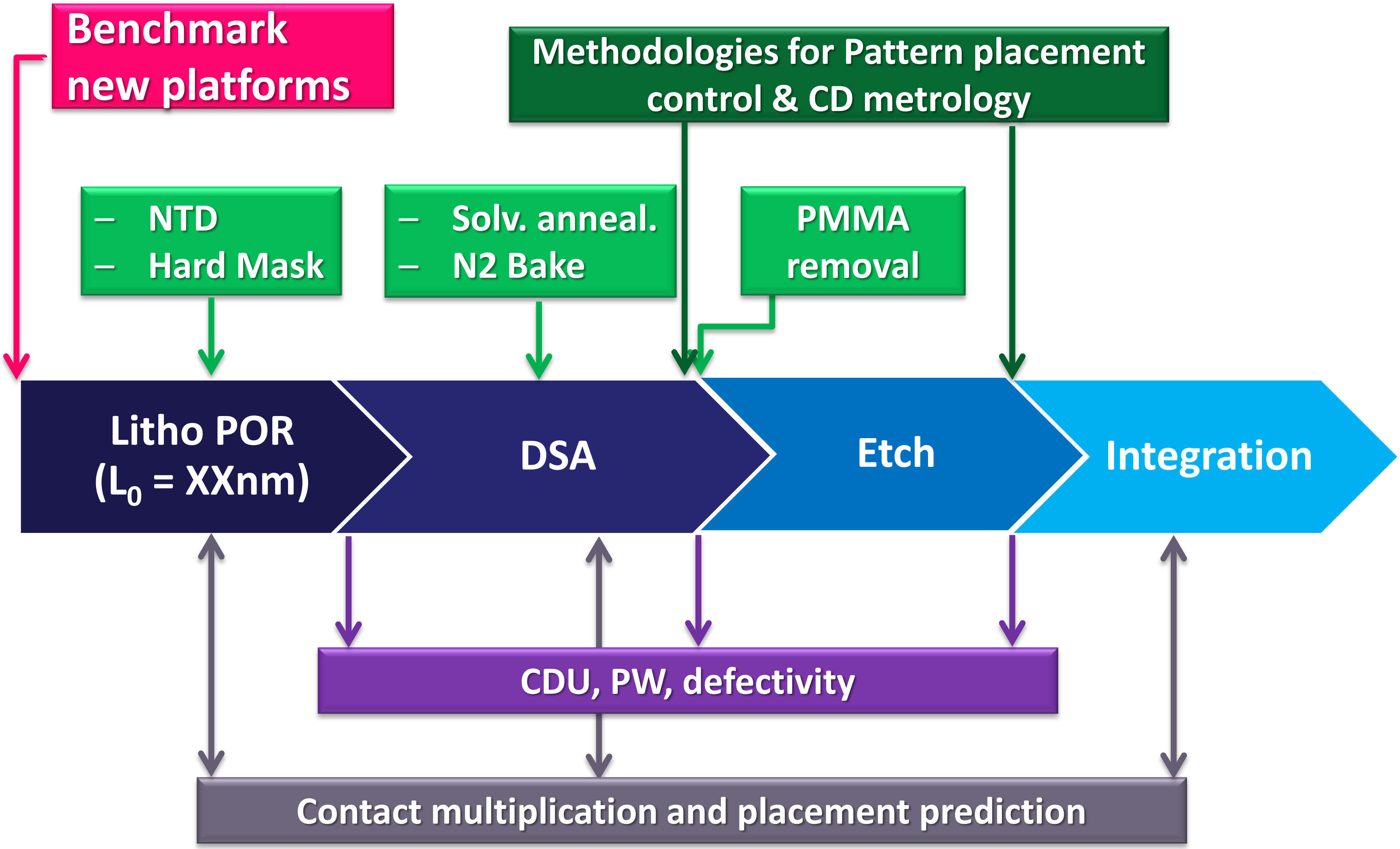
Overview on IDeAL scope of work



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Summary of technical achievement

- DSA is a complementary lithography technique
  - In a first step by using PS-b-PMMA like materials (lowest CD after etching 10nm); In a second step by using high χ materials

- A credible alternative for contact and via patterning
  - CDU is improved by using DSA $3\sigma < 2$nm
  - Defectivity 5 defects per wafer (99.97% of good contacts): need to move to automatic measurements
  - Etching capabilities demonstrated
  - Metrology DSA is in film order: need to implement hybrid approach

- What's next: 2D structures
  - Physical and compact models have to be implemented in order to predict order

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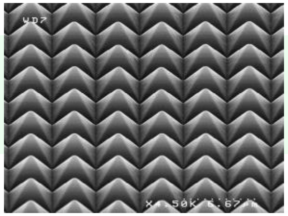
Lithography options for tomorrow

- Optical lithography
  - 193nm
  - EUV
- E-Beam direct write lithography
- Self Aligned Ligraphy by block copolymers
- Imprint lithograhy



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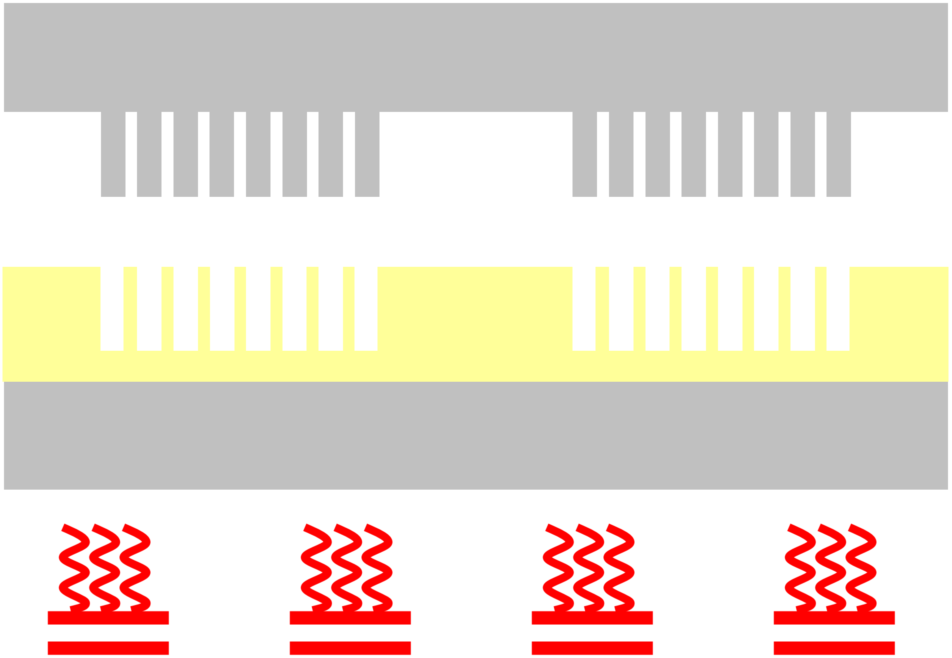
The technology



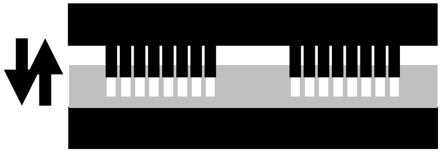
Hot Embossing

proposed by Chou in 1995

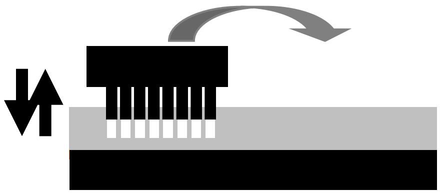
UV Imprint

proposed par Colburn & Wilson in 1999

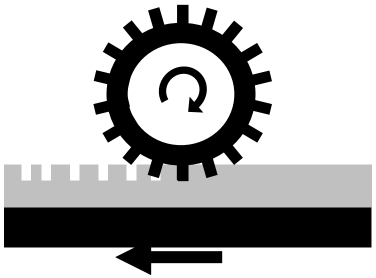
Nano-Lithography, *Stefan Landis*, ISTE-Wiley, December 2010, 352 pp



Full wafer Imprint



Step and Stamp



Roller imprint

- More than Silicon substrates
- Polymer / flexible substrates
- Bio compatible polymers
- High resolution / large surface
- 3D complex shapes
- Non flat samples

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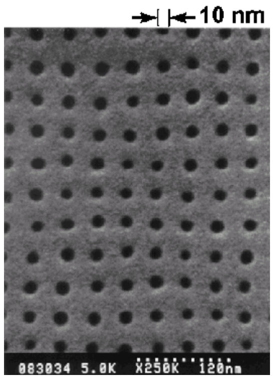
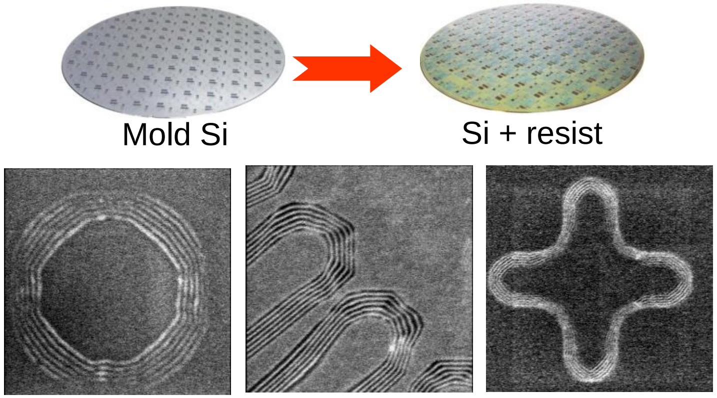
IMPRINT capabilities

1995 (U. Minesota)



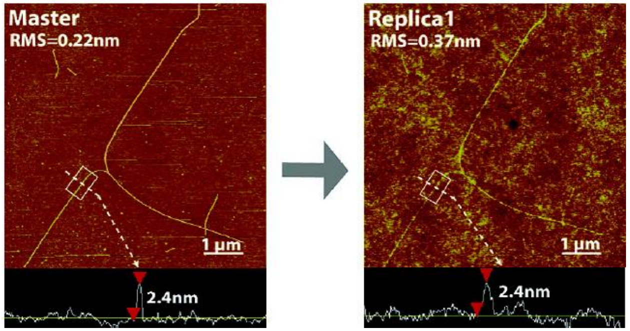
⇒ Very high resolution
⇒But on a few µm²

2003 (CEA-LETI)



⇒ Large surface (200 mm wafer)
⇒ Very high resolution (10 nm /10 nm)

2004 (U. Illinois)

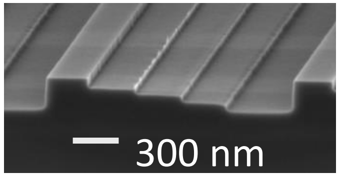


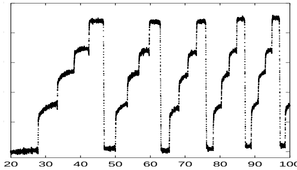
⇒ Molecular Scale resolution : resolution 2 nm

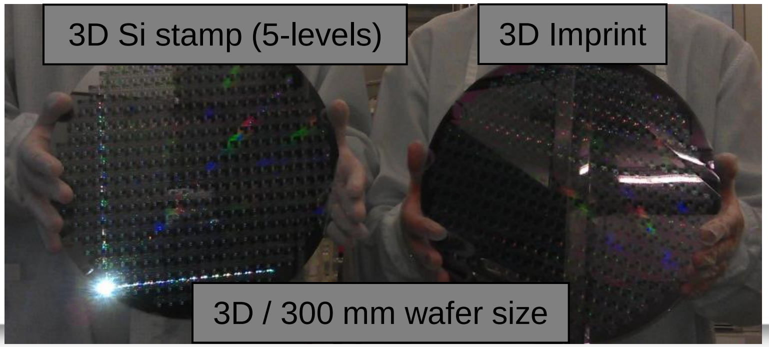
2004 ➔ 2011

⇒ Introduction in ITRS (2005) / Industrial players
⇒ Equipment (sub 30 nm alignment accuracy, size enlargement, throughput improvement)
⇒ Process (stamp manufacturing, functional materials, lower defectivity)

2012 (CEA-LETI)







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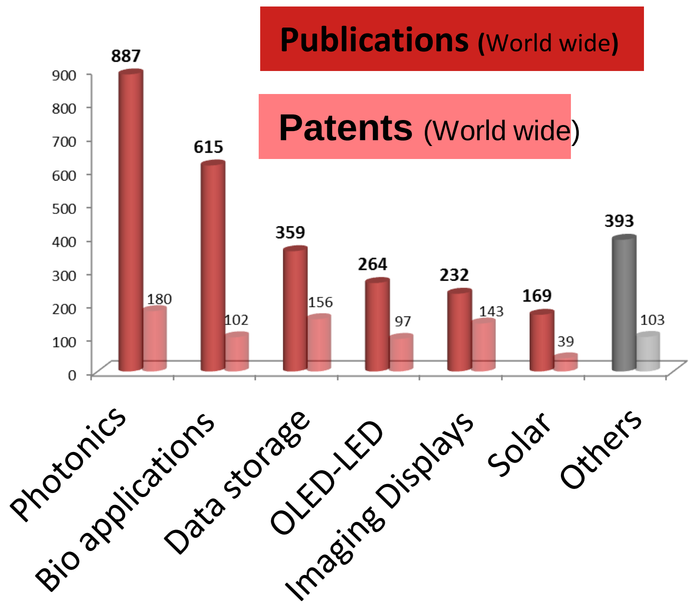
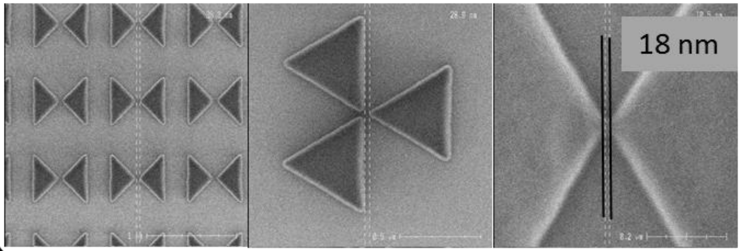
Focus on CEA-LETI activities



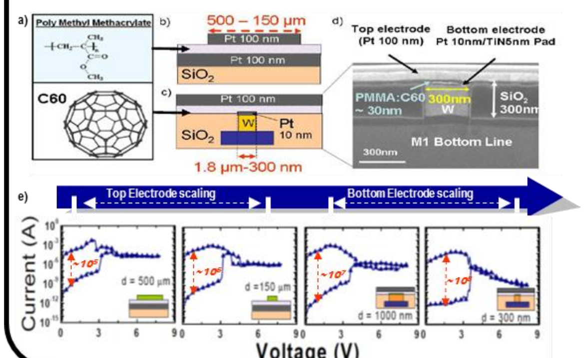
BIO APPLICATION

Imprinted bow ties (on 200 mm wafer)

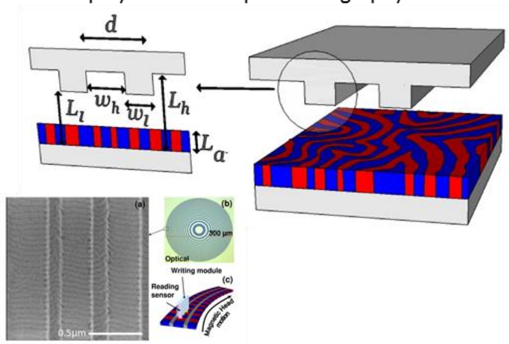


DATA STORAGE

Direct patterning of Organic resistive memories with C60 molecules embedded in PMMA

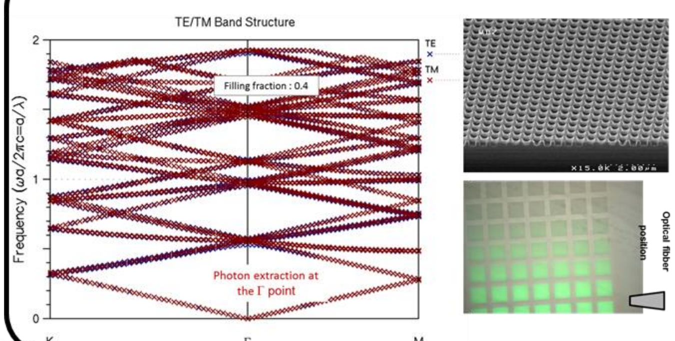


Tailoring Nanostructures Using Copolymer Nanoimprint Lithography

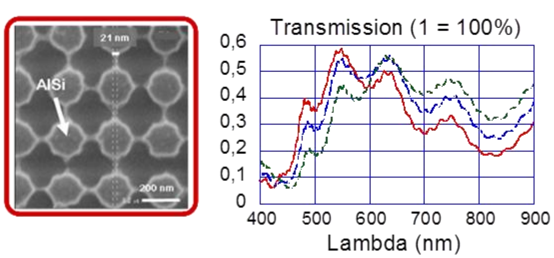


PHOTONICS

Photonic Crystal for light extraction



Metallic color filters



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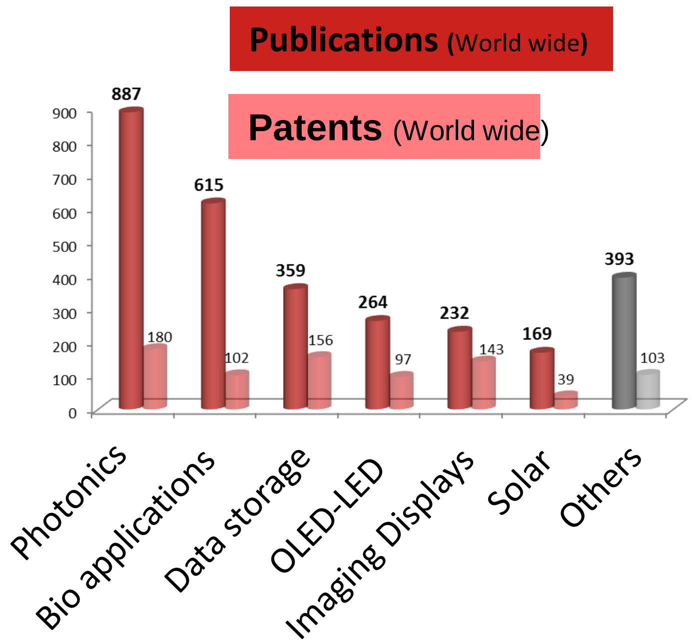
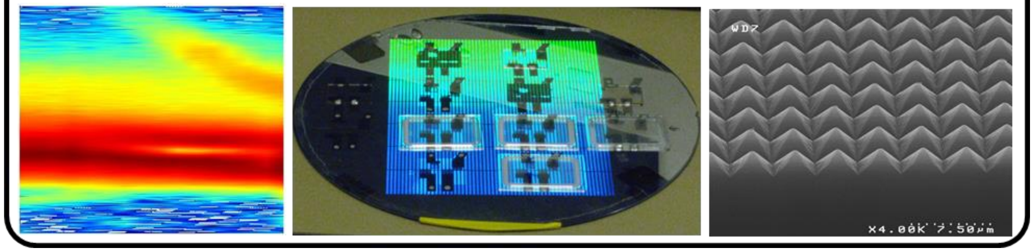
LETI demonstration works



OLED-LED

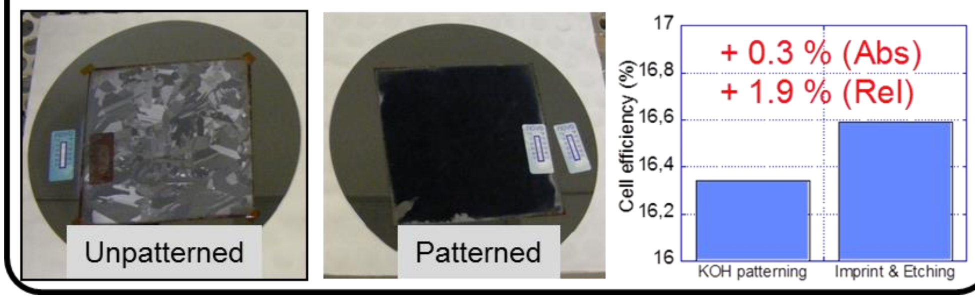
Electro Optical characterization +20% of light

PSS for LEDs



SOLAR

Multi crystalline Si solar cell patterned with NIL processes

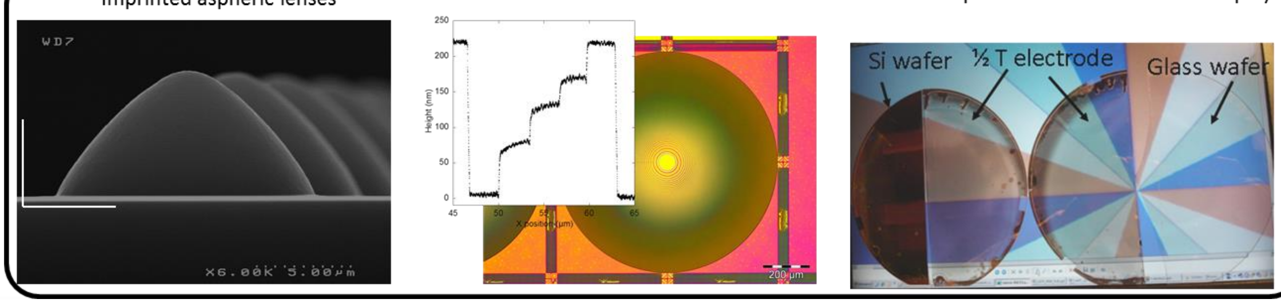


IMAGING-DISPLAY

Imprinted aspheric lenses

3D Fresnel lenses

Metallic ½ transparent electrode for OLED display



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To conclude…

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Acknowledgments

- LETI team
  - The **entire** lithography laboratory
    - Special thanks : R Tiron, B Icard, J. Belledent, C Constancias
    - BelledentS Tedesco, Y Trouiller, S Landis
- MAPPER
  - MAPPER team @ LETI : P Wiedemann, A Farah
  - MAPPER Delft : BJ Kampherbeek… and the 199 other employees !
- ARKEMA
  - X Chevallier, C. Navarro, M Argoud, I Cayrefourcq
- LCPO
  - G Hadzianou and the LCPO team
- INTEL
  - Y Borodowsky

Contact : laurent.pain@cea.fr

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Which lithography for tomorrow? Look in the crystal ball

- 4 choices
  - 193nm & double exposure

    Reliable and mature technology facing resolution capability limits
  - EUV : photon forever

    High development cost>2B$... Still not mature…
  - Multibeam

    Potential is here, but no sufficient support from IDM world
  - DSA
    - Smart option with rising interest… but need to progress
  - Imprint
    - Interest **YES**… but overlay and defectivity issues for CMOS applications

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DO your own market !

- A lot of possible options and combinations
  - Photons or electrons
  - Single or multiple

- Who will be the winner
  - The solution on time
  - The most cost effective one
  - The one compatible with design requirements

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Few words on LETI collaborative dynamic

The LETI environment IS OPEN to push collaborative programs

Partnerships with
- Industry
- Academics

Metrology

Modelling
EPC, DSA model

Data extraction & calibration

LETI open positions 2013-14
→ 2 Ph D students
→ Trainees
→ Post docs

ONE OBJECTIVE FOR ALL : Develop soluti

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leti

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DE L'INFORMATION

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Thanks for your attention

Questions

- What is the cost of 1 million transistor in 2009
  - 1 - 1$
  - 2 - 0,1$
  - 3 - 0,01$

- Howmany litho steps are needed to manufacture an IC?
  - 1 - 40-60
  - 2 - 40-50
  - 3 - 20-40

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QUESTIONS

- What is the minimum achieveable k1 process factor of optical lithography
  - 1 – 0.33
  - 2 – 0.25
  - 3 – 0.22
- What is the resolution limit of a 193nm 1.35NA tool based on Rayleigh criteria in single exposure mode?
  - 1 – 40nm
  - 2 – 35nm
  - 3 – 32nm

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QUESTIONS

- What is the triangle of death of resist process development
  - 1 – Resolution – sensitivity – roughness control
  - 2 – Resolution – sensitivity – mechanical& chemical stability
  - 3 - Resolution – sensitivity – etch selectivity
- What are the possibility to improve k1
  - 1 - Resist exposure optimization
  - 2 - OPC
  - 3 - Illumination modification

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Questions

- Key concerns of EUV lithography today
  - 1 – Source power
  - 2 – Scanner reliability
  - 3 – Mask infrastructure
  - 4 – Resist resolution
  - 5 – Resist sensitivity
  - 6 - Optic reliability
- Advantages of low accelerating voltage E-Beam direct write lithography?
  - 1 - Low charging
  - 2 - Heating
  - 3 - Resolution
  - 4 – Throughput
  - 5 – CD uniformity control

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Questions

- Advantages of tri-layer stack for low accelerating E-Beam ditrect write lithography?
  - 1 - Resolution
  - 2 - Charging
  - 3 - Heating
  - 4 - Roughness
  - 5 - Sensitivity
  - 6 - Reduction of back scattered electron level
- What is the link between resolution and intrinsic period of block-copolymer?
  - 1 – intrinsic period = resolution limit
  - 2 – intrisic period = ½ resolution limit
  - 3 – No relationship between resolution and intrinsic period

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Questions

- What is the intrinsec L0 range achievable so far with PS-PMMA platform
  - 1 - 10nm < L0 < 120nm
  - 2 - 10nm <L0 < 60nm
  - 3 - 20nm < L0 < 60nm
  - 4 - 20nm < L0 < 120nm
  - 5 - Basically no limitation. It depends of polymer molecular weight parameters
- Key advantage(s) of DSA solution
  - 1 – Throughput
  - 2 – Resolution
  - 3 – Pitch reduction
  - 4 – Roughness limitation
  - 5 – Design rule simplicity
  - 6 – Technology cost reduction (including all manufacturing steps)

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Questions

- What is THE key advantage of Imprint lithography ?
  - 1 - Defectivity
  - 2 - Throughput
  - 3 - Resolution
  - 4 - Overlay
  - 5 – All these parameters
- What is the key application today for imprint lithography based on publication and patent ranking ?
  - 1 - Bio systems
  - 2 - Data storage
  - 3 - Photonics

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