Nano-devices

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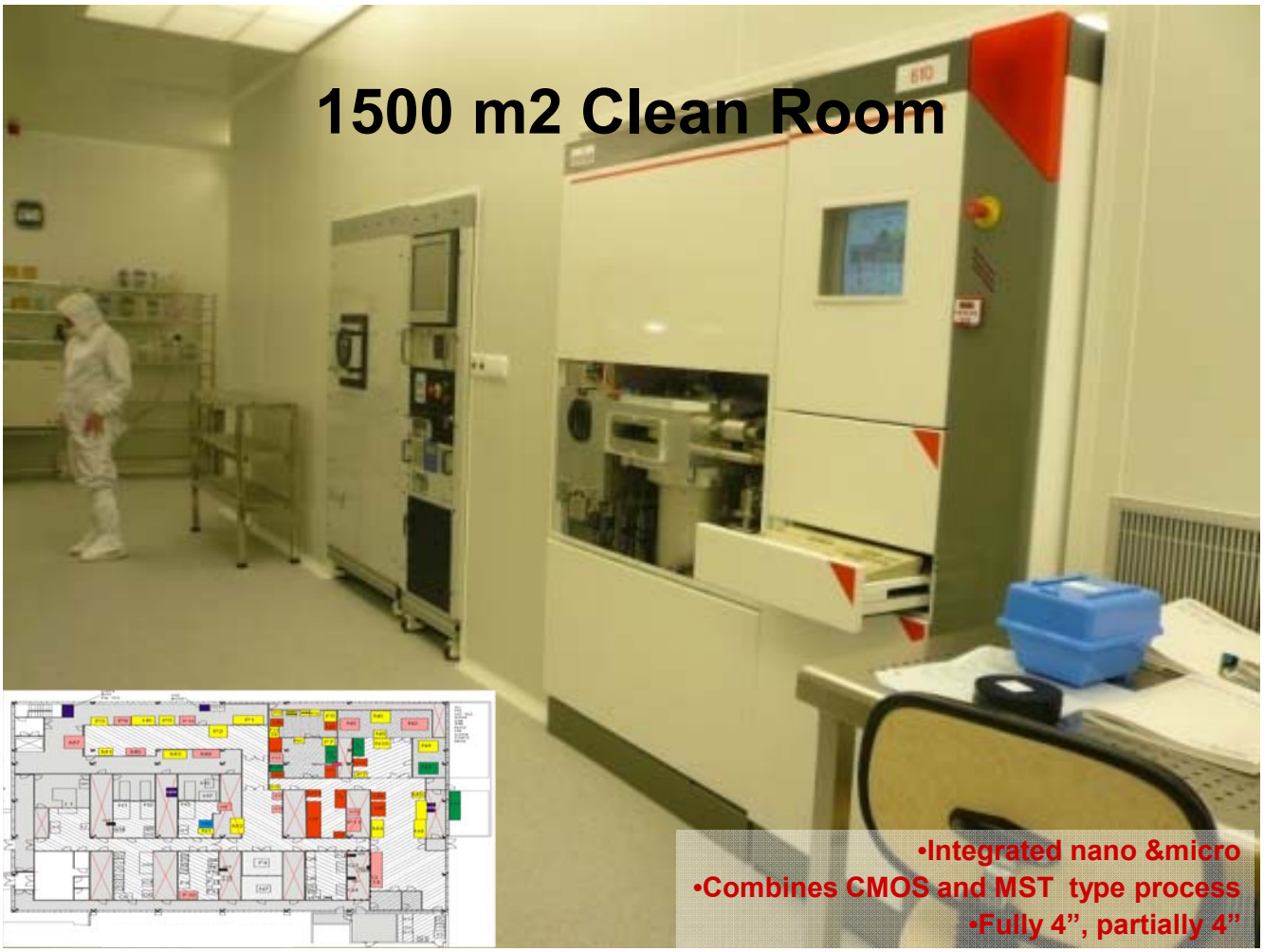
Más...
Mapa
Satélite
Relieve
Barcelona
2 km


Más...
Mapa
Satélite
Relieve
UAB CAMPUS
200 m

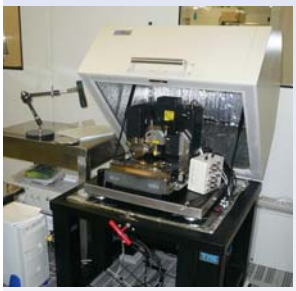
1500 m2 Clean Room



- Integrated nano &micro
- Combines CMOS and MST type process
- Fully 4", partially 4"

Nanolithography equipment

AFM



e-beam writer

UV-Nanoimprint

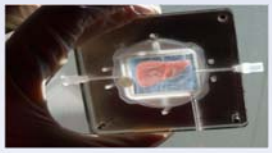
365 nm

SEM

FIB (Dual beam)

Thermal NIL

Value chain in Nanoelectronics

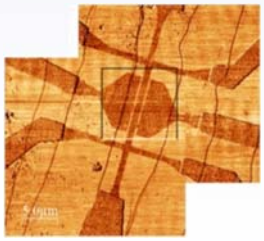


Safety and environmental monitoring

Health

Energy management and harvesting

Digital industry and IOT



Materials, process and integration

OUTLINE

- Why nanodevices
- Limits of optical lithography
- Directed Self-assembly of block copolymers
- FIB implantation for nanodevice fabrication

Why reducing the dimensions of a device?

- Advantages:
  - **Speed (fast response time) / Sensitivity**
  - **Less energy consumption**
  - Save of space/Increase of integration
  - Save of material cost / Batch fabrication

- Scaling:
  - Need for adapted fabrication methods
  - At micro and nano scale, objects behave differently
    - Macroscopic scale: Water falls down from a glass facing down
    - Microscopic scale: Due to surface tension, water does not fall down from a glass facing down

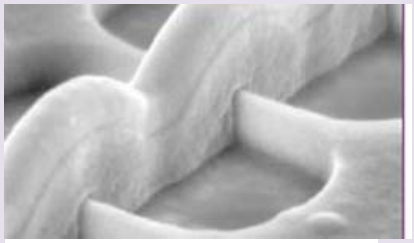
Miniaturization in electronics:

The technology that has most influenced life during the last 60 years

Computers

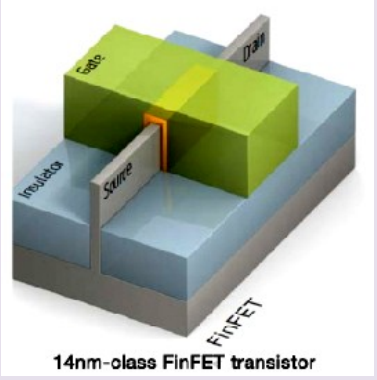
Communication

Entertainment



The Transistor

Miniaturized Switch



14nm-class FinFET transistor

Some features:

- Transistor Fin Pitch: 42 nm
- Transistor Gate Pitch: 70 nm
- Interconnect Pitch: 52 nm
- 0.0588 um^2 SRAM cell
- Approx: 10 billions transistors /microprocessor
- Frequency: 4 GHz

THE NANO DEVICE !!

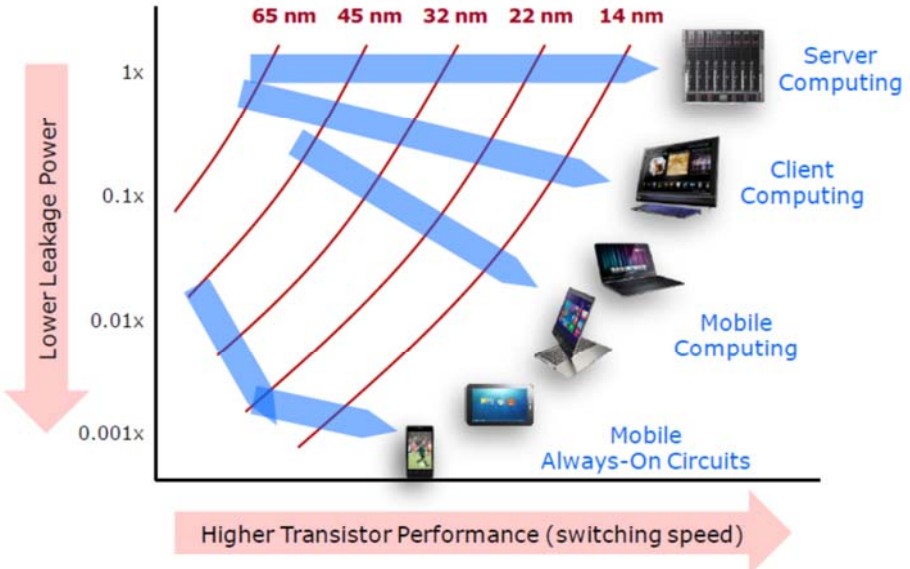
Dimensions: 10 nano-metres

Switching time: 0.1 nano-seconds

Number of transistors: 10^9

Power consumption

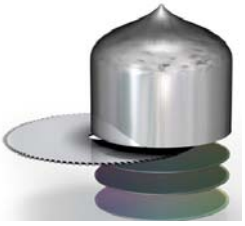
Transistor Performance vs. Leakage



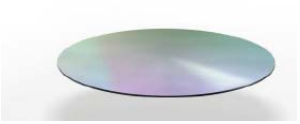
How integrated circuits are fabricated?

Sand

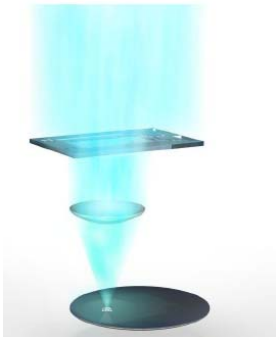
Silicon crystal growth

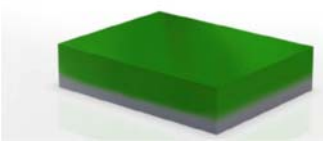


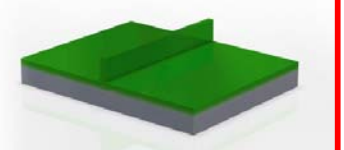
Slicing



Wafer
(300 mm diam.,
<1 mm thick)

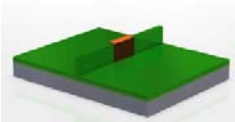




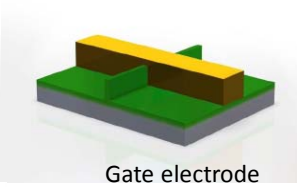


Material deposition /growth

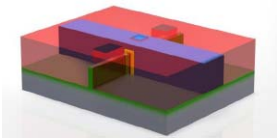
Lithography + etching



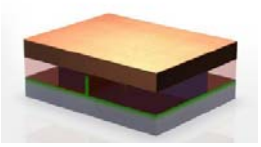
Gate oxide



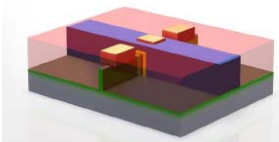
Gate electrode



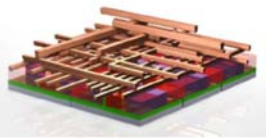
Insulation bottom level



Metallization

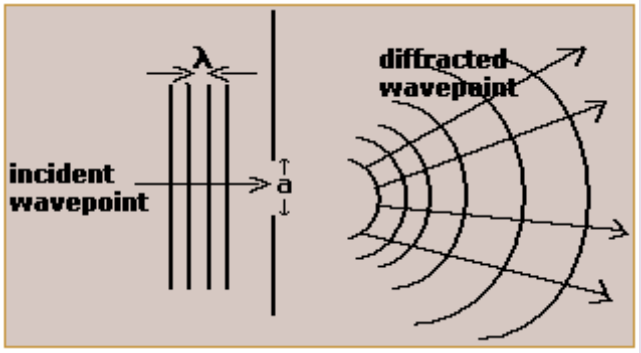


Electrical contacts



Multiple-level contact

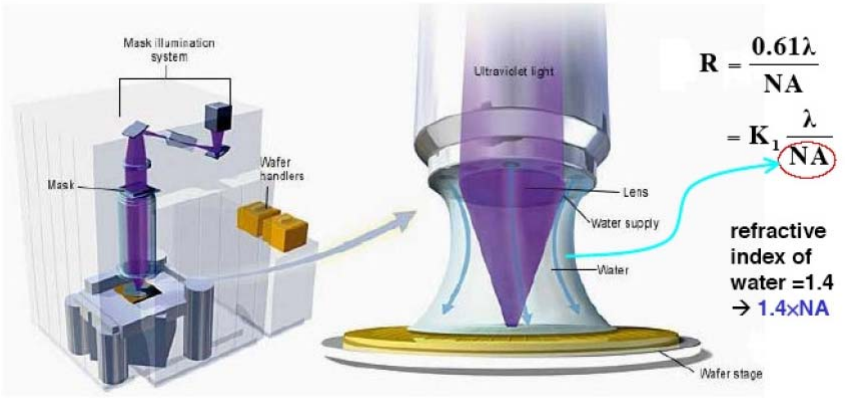
Diffraction limits resolution



$$R = k1 \frac{\lambda}{NA}$$

K_1=0.22, λ= 193 nm, NA=1.35 ⇒

Resolution= 32 nm



Today's lithography equipment

Price: approx 100 M€

Double patterning techniques

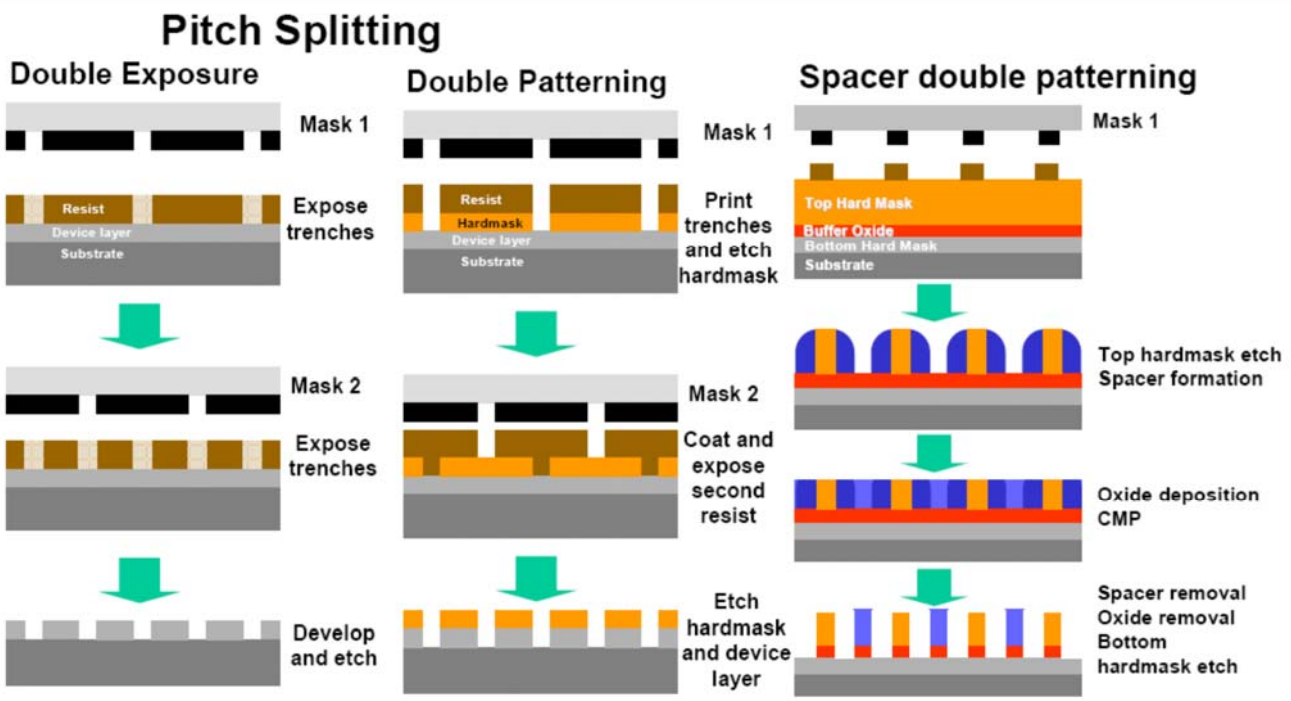
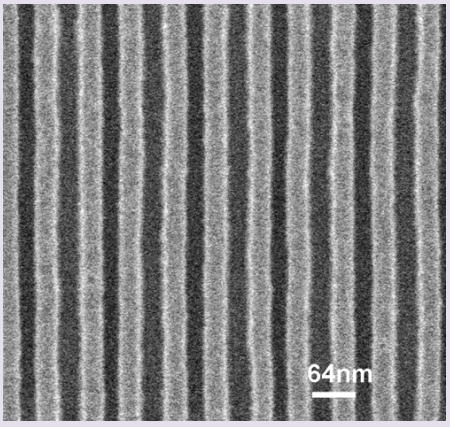


Figure LITH1 Process Flows for Pitch Splitting (DE, DP), and Spacer Patterning

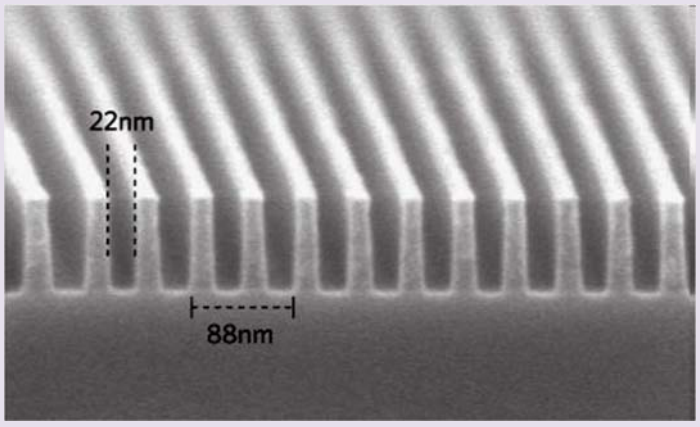
11 nm channgel length achievable with immersion lithography

Double patterning techniques



32nm half-pitch poly-Si gates etched using double pattering

© IMEC



Self-aligned double patterning 22 nm half pitch

© Applied Materials

EE Times Connecting the Global Electronics Community

News & Analysis

EUV in Final Push into Fabs

Making progress amid 'a lot of pressure'

Rick Merritt
5/29/2018 02:01 AM EDT
9 comments

NO RATINGS
LOGIN TO RATE

Like 28 Tweet Share G+

ANTWERP, Belgium — A 20-year struggle to launch a next-generation lithography tool has entered its final phase as engineers race to unravel a rat's nest of related issues. Despite complex problems and short deadlines to bring extreme ultraviolet (EUV) steppers into high-volume manufacturing, experts remain upbeat.

The good news is that many shoulders are pushing the wheel ahead. "In the past, one company would take a lead with a new semiconductor technology, but now all the logic guys are jumping in, biting the bullet, and taking the risks," said An Steegen, executive vice president of technology and systems at Imec.

The research institute in Belgium is a long-standing collaborator with ASML, the developer of EUV in the Netherlands. Together with foundries and suppliers, they now aim to work out the last major kinks in the room-sized systems that will print next-generation chips.

It's like when the FinFET transistor emerged in 2008 as a significant but challenging vehicle for new performance gains, said Steegen in an interview at the Imec Tech Forum here.

"People compared the worst case of next node to the best case of the old node, but now all sides agree that FinFETs are extremely high-performance devices. My lesson is to take it all with a grain of salt … there are enough features ahead to deliver improvements so that SoC designers get what they want."

In a separate, informal conversation waiting in line for coffee at Imec's headquarters, a 32-year veteran working on EUV put it simply: "There are a lot of pressures right now … but we are making progress."

Indeed, Samsung's foundry is racing to get EUV into production at 7 nm before the end of the year. It aims to pull ahead of larger rival TSMC, which is taping out many 7-nm chips now using existing immersion steppers.

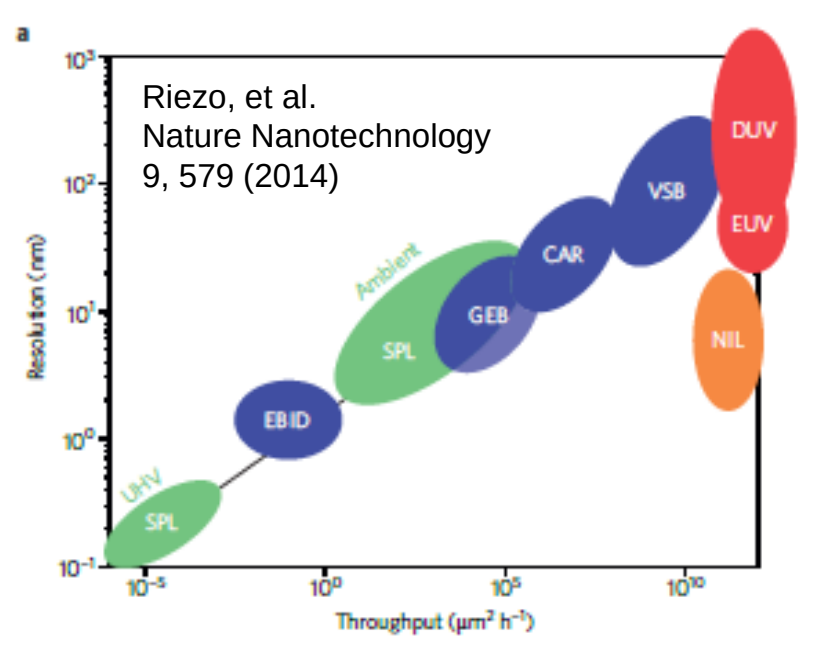
TSMC and GlobalFoundries are not far behind, aiming to ramp enhanced 7-nm nodes with EUV early next year. Separately, Imec estimates that DRAM makers will adopt EUV for their D14+ nodes — probably in 2021, when half pitches dip below 20 nm.

Two of Imec's current focus areas are helping to smooth out line-edge roughness and eliminating so-called stochastics, random errors that create missing or kissing contacts. The errors were first reported earlier this year at 15-nm dimensions key for a next-generation 5-nm node, but researchers now say that they also see them at 7 nm.

Steegen expects that hybrid solutions will emerge. They will use a combination of scanner settings, resist materials, and post-processing techniques that stitch broken lines, smooth jagged ones, or fill out missing contacts.

Foundries can apply higher doses of EUV light — say, 80 millijoules/cm^2 — to widen a process window, but that will slow throughput. "Deciding the peak dose for the first implementations is up to the foundries," said Steegen.

Nanolithographies: Present status



SPL: Scanning Probe Lithography

EBID: Electron Beam Induced Deposition

GEB: Gaussian Beam Electron Beam Lithography

CAR: Chemical Amplified Resists Electron Beam Lithography

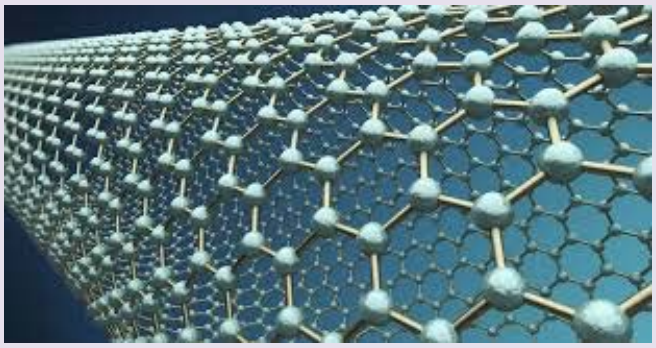
VSB: Variable Shape Beam Electron Beam Lithography

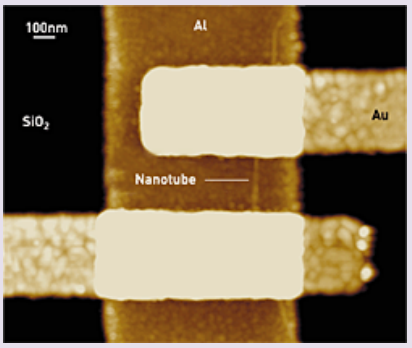
DUV: Deep UV Optical Lithography

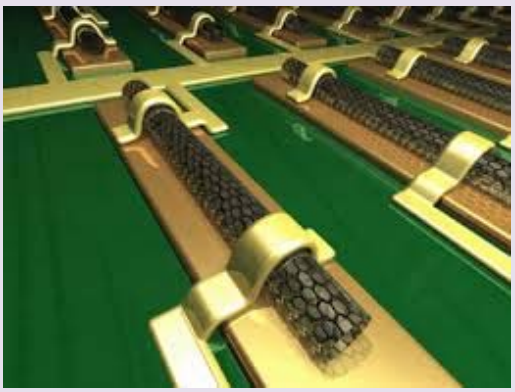
EUV: Extreme UV Optical Lithography

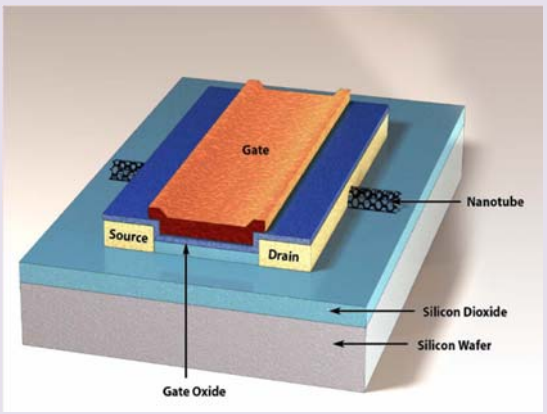
NIL: Nanoimprint Lithography

Bottom-up fabrication









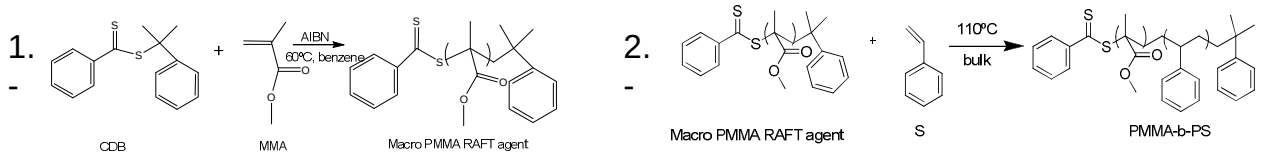
DSA

DIRECTED SELF-ASSEMBLY OF BLOCK CO-POLYMERS

BLOCK CO-POLYMER

Block copolymers are a specific class of copolymer (polymers comprising more than one chemically distinct monomer) where the different monomers are not distributed within the polymer chain in random or alternating fashion but instead are grouped in discrete homogeneous sections (or blocks) of the chain.

Conceptually a block copolymer can be thought of as two or more distinct homopolymers linked end to end through covalent bonds. The number of distinct homopolymer homogeneous sections determines the molecular architecture of block copolymer; diblock, triblock, and higher multiblock copolymers are possible



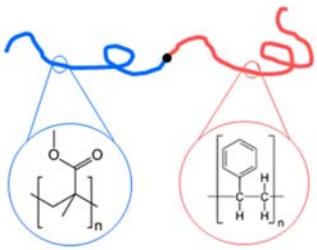
A = methyl methacrylate B = Styrene

PMMA-b-PS

Ho-Cheol Kim, Sang-Min Park, and William D. Hinsberg. **Block Copolymer Based Nanostructures: Materials, Processes, and Applications to Electronics. Chem. Rev. 2010, 110, 146-177**

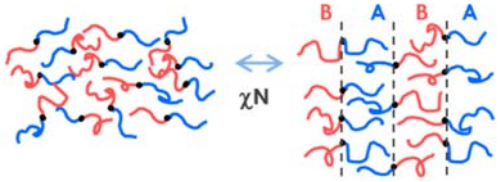
Phase separation in block copolymers

Just as most polymer mixtures will separate into different phases, the two blocks of a diblock copolymer tend to demix. The covalent bond linking the blocks, however, prevents the macroscopic phase separation observed in binary mixtures of the homopolymers and results in nanoscale structural organization of each block.



Disorder-order transition

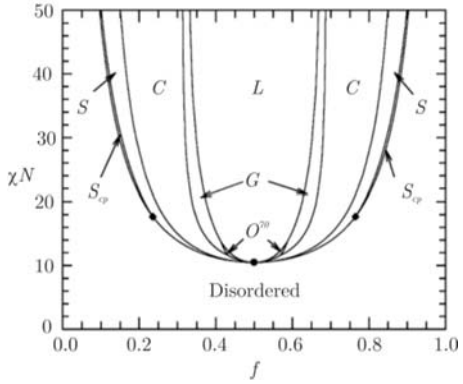
f: Volume fraction of one block in a BCP
N: Polymerization index
χ: Flory-Huggins interaction parameter



Phase separation in block copolymers

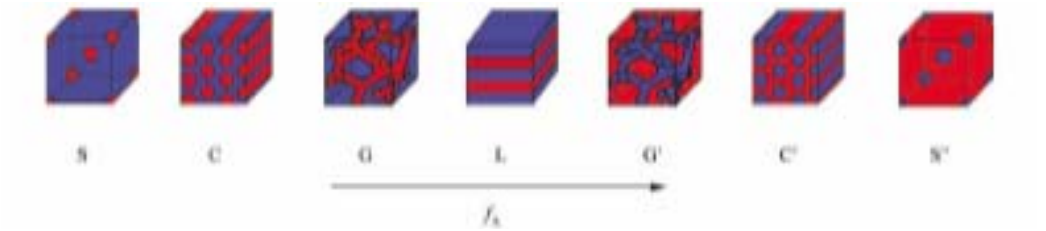
- The propensity for block copolymers to phase separate into periodic microdomains is determined by the strength of the repulsive interaction

- It is characterized by the product χN:
  - χ is the Flory-Higgins interaction parameter
  - N is the number of monomers in the diblock copolymer

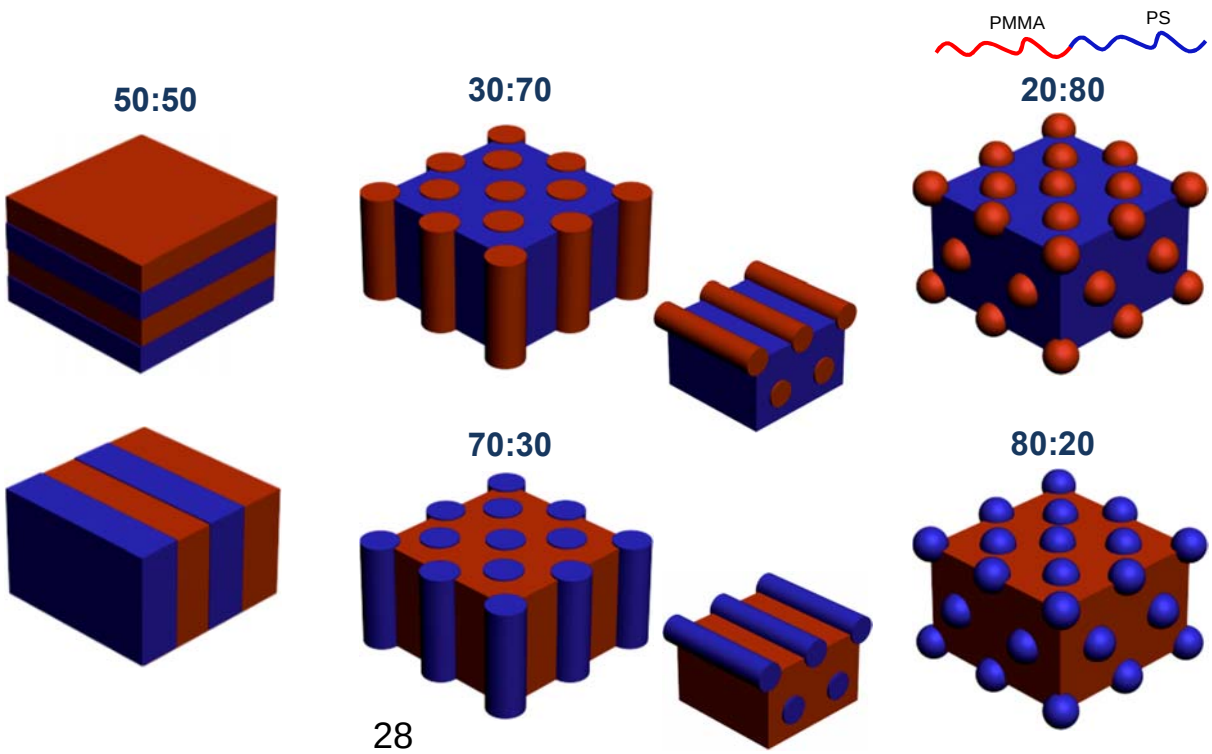


- Microphase separation can occur when χN exceeds the critical value for the order-disorder transition.

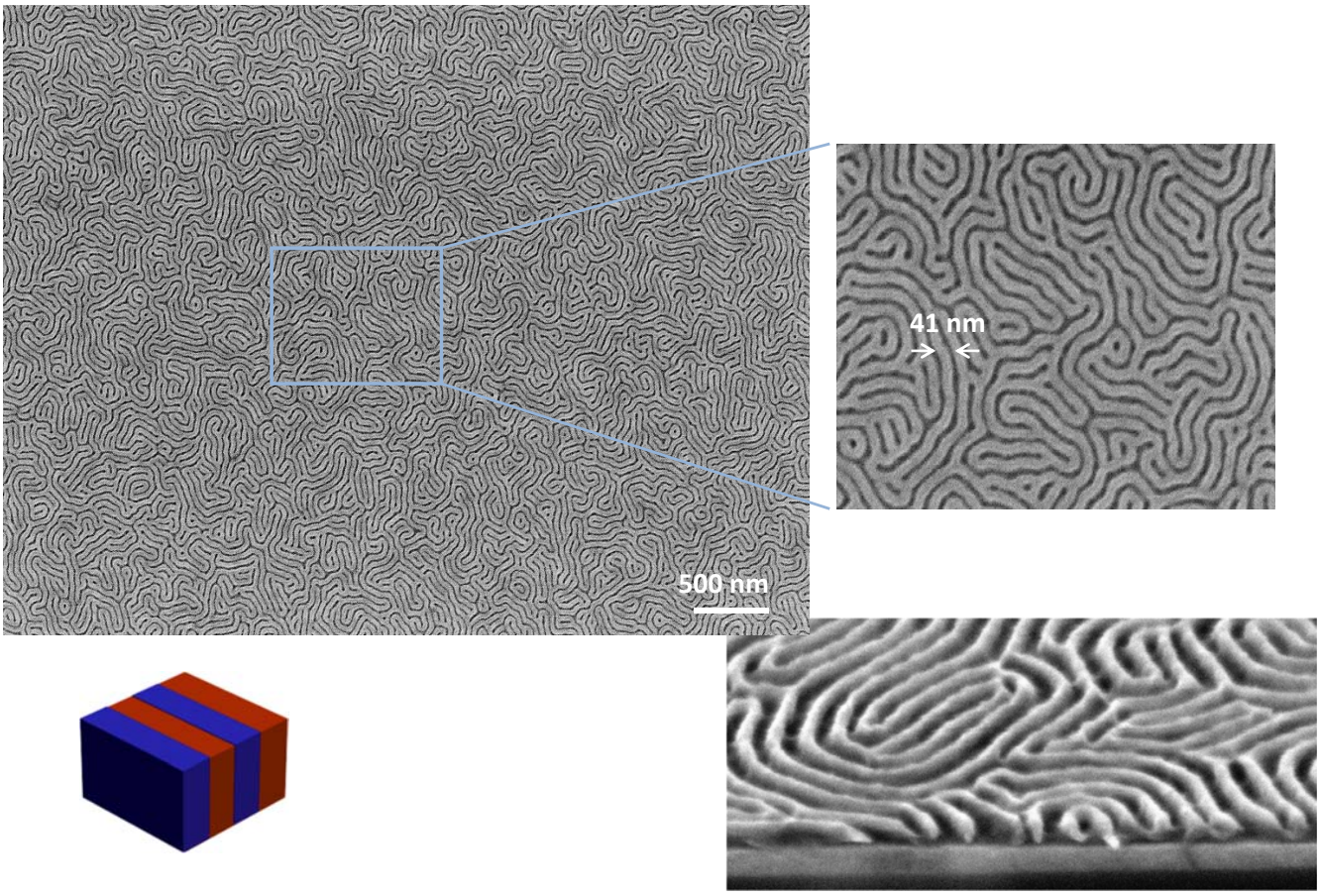
- At equilibrium, this microphase separation is established by the energy balance between the stretching energy for the polymer chains and the energy of interactions at the interface between A and B microdomains.



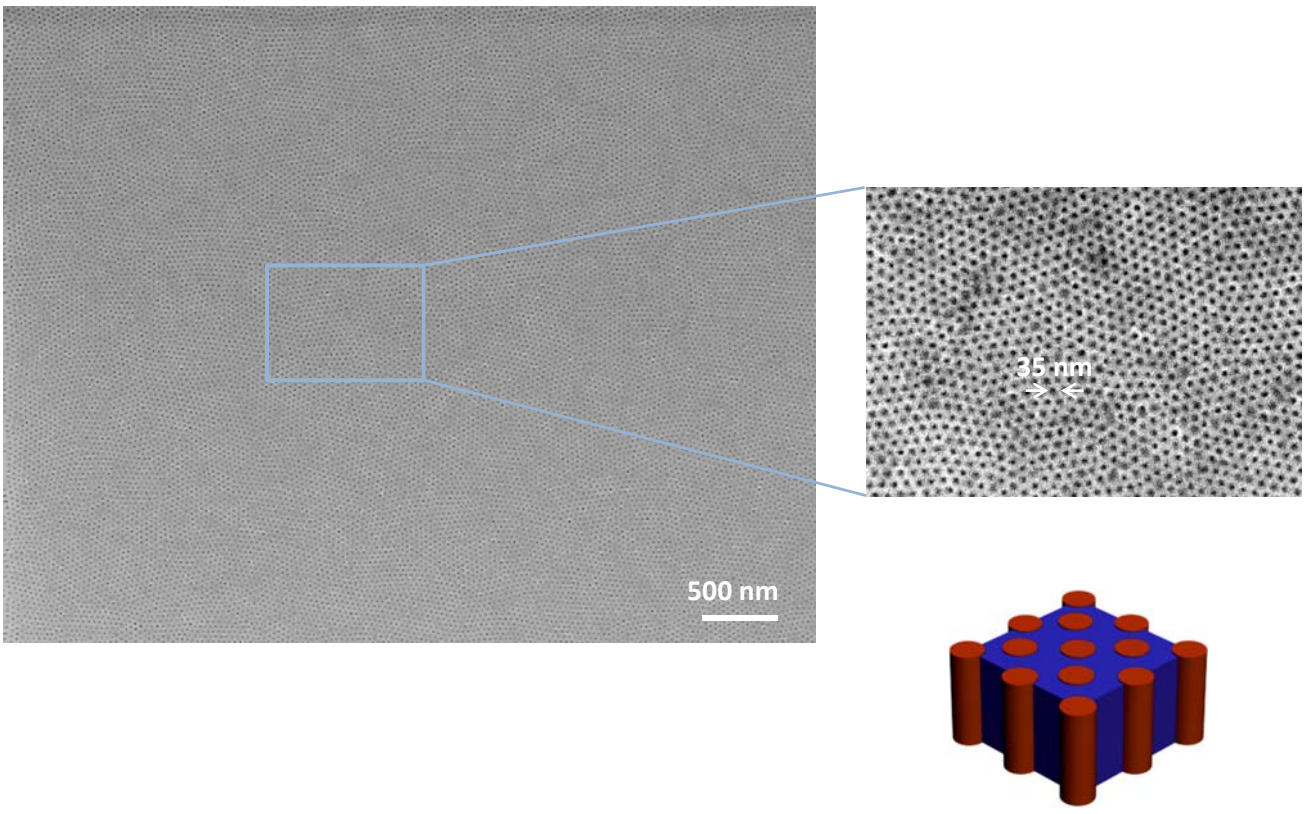
PHASE SEPARATION AND SURFACE/INTERFASE ENERGY



Examples of phase segregation

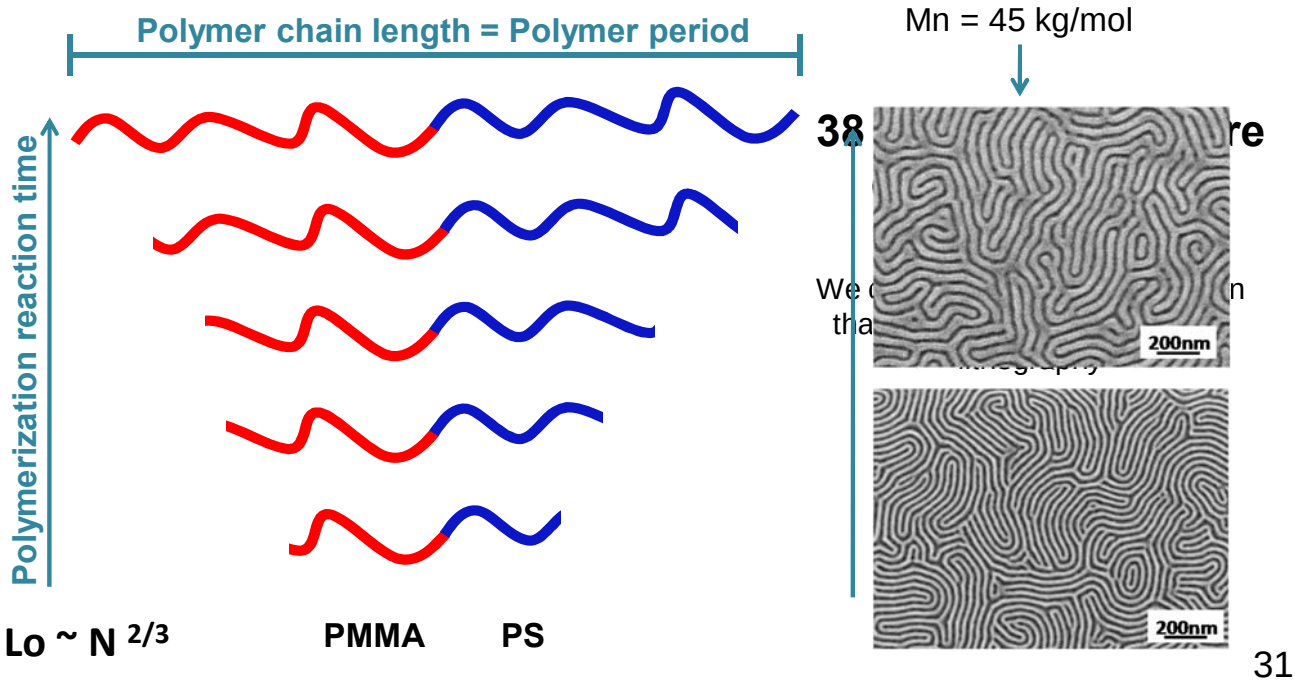


Examples of phase segregation

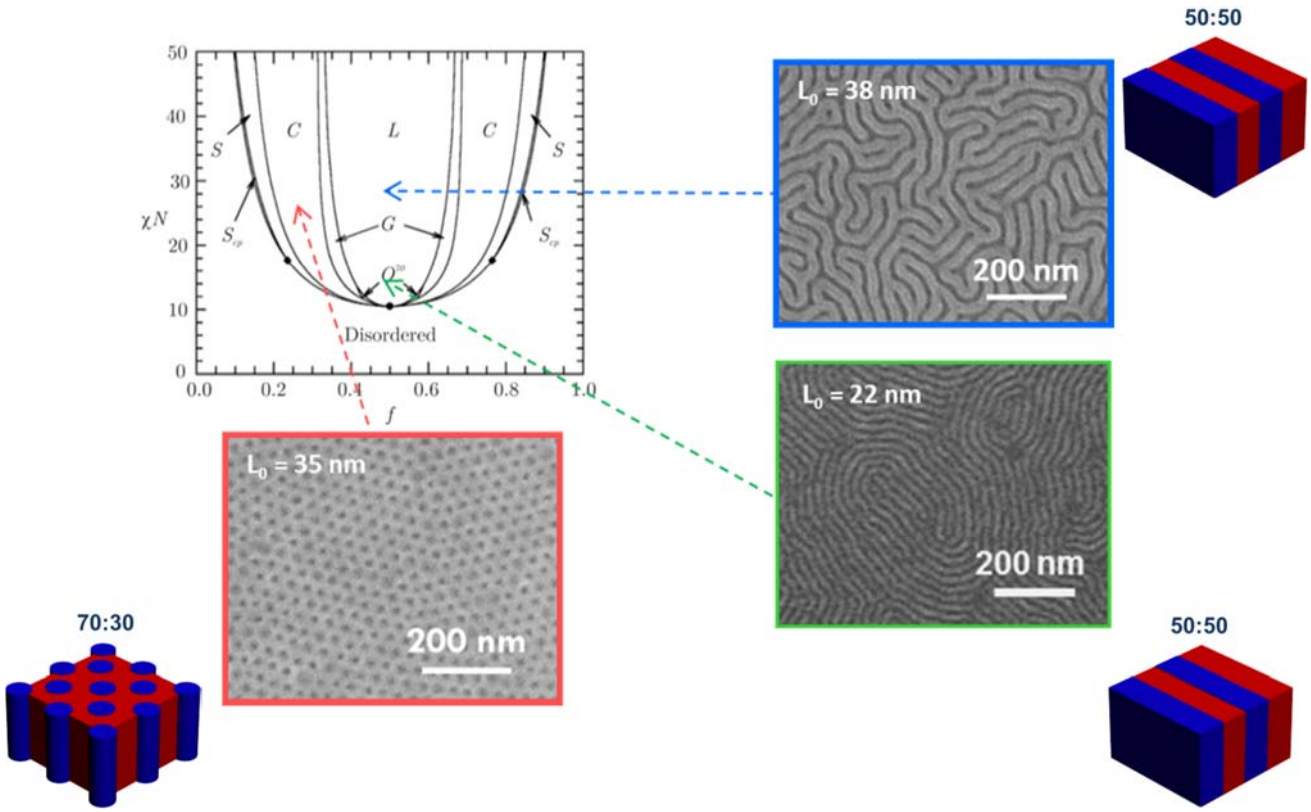


BLOCK CO-POLYMER SELF-ASEMBLY: HALF PITCH SIZE SETTING

The pitch we obtain depends on the molecular weight and the CD uniformity depends on the polidispersity index



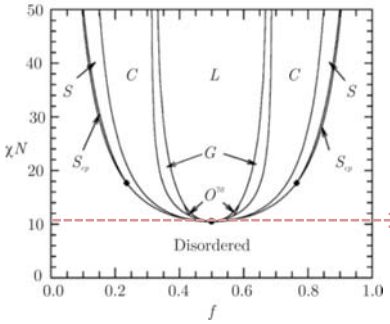
Morphologies of diblock copolymers



Bates, F.S. and Fredrickson, G.H. "Block copolymer thermodynamics: Theory and experiment", *Annu. Rev. Phys. Chem.*, 41 (1990)

High-χ block co-polymers

Development of **new DSA processes** and materials to scale to **5 nm** with potential to fulfill the future requirements of microelectronics industry



PS-*b*-PMMA
χ ≈ 0.04
↓
Resolution limit to 11 nm

High- χ materials requirements

- High χ
- Good etching selectivity
- Mechanical stability
- Orientation control and alignment availability with low defectivity

Organic high- χ materials
- Low etching contrast between blocks
- Not very high- χ values

Inorganic high- χ materials
- High etching contrast between blocks
- High- χ values

Organic BCPs		Inorganic BCPs	
BCP system	χ value	**BCP system**	χ value
PS-b-PMMA	0.041	**PS-b-PFS**	0.08
PS-b-PEO	0.077	**PS-b-PDMS**	0.26
PS-b-P2VP	0.178	**PTMSS-b-PLA**	0.46
PS-b-PLA	0.233	**PS-b-MH**	0.58
PS-b-PI	0.110	**PLA-b-PDMS-b-PLA**	1.4

Each block copolymer requires the proper neutralization layer

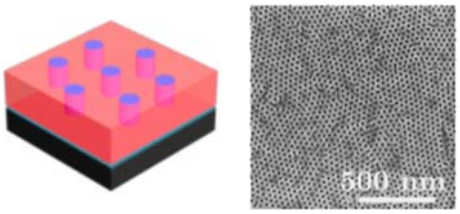
Block copolymers in thin films

$$F = (F_{A/B} + F_{conf}) + (F_{A/Subs} + F_{B/subs} + F_{A/air} + F_{B/air})$$

Interaction energies

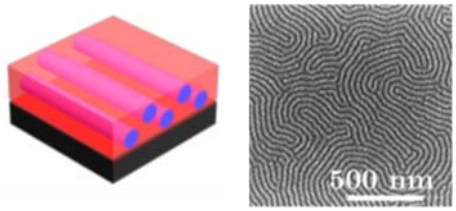
Role of surface affinity

Neutral surface



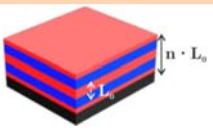
$\gamma_{A\text{-air}} \approx \gamma_{B\text{-air}}$
$\gamma_{A\text{-subs}} \approx \gamma_{B\text{-subs}}$

Affine surface

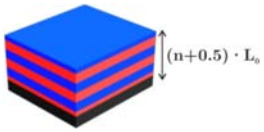


Role of block copolymer film thickness

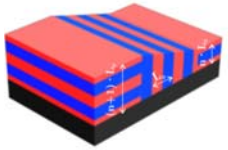
$\gamma_{A\text{-air}} < \gamma_{B\text{-air}}$
$\gamma_{A\text{-subs}} < \gamma_{B\text{-subs}}$

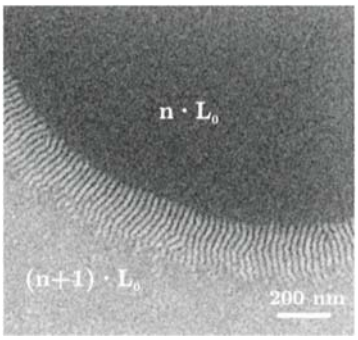


$\gamma_{A\text{-air}} > \gamma_{B\text{-air}}$
$\gamma_{A\text{-subs}} < \gamma_{B\text{-subs}}$



When the BCP **does not** fulfill the film thickness **commensurability** condition, the BCP tend to create some **holes** or **terraces**

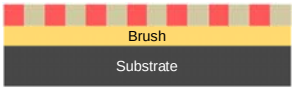




Interface neutralization

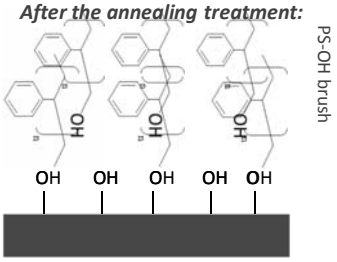
For technological applications there is the need to control the BCP morphology, and thus **avoid wetting morphologies** at the polymer-brush interface.

Use of **brush polymer** to create a neutral layer which balances the surface free energy between the BCP domains

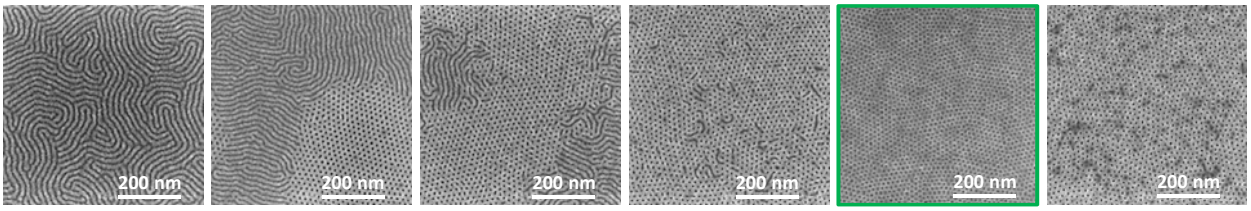


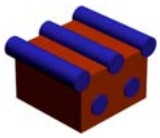
Mansky, P., "Controlling polymer-surface interactions with random copolymer brushes", Science, 275, 1458-1460 (1997)

After the annealing treatment:



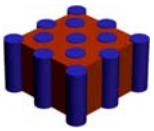
% PMMA (PS-r-PMMA)





SEM images taken after PMMA removal

Cylindrical PS-b-PMMA.



Thin film preparation of block co-polymers

1. Preparation of a surface with the proper interface energy (usually , deposition of a monolayer of molecules)
2. Dissolution of the co-polymer in a solvent
3. Spinning of the solvent
4. Annealing (Thermal annealing or solvent annealing)

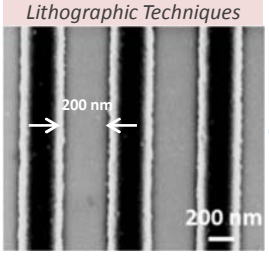
Annealing increases the mobility of the copolymer molecules, so the film can more rapidly reach its final structure.

In thermal annealing the sample is held at a temperature above the glass transition temperatures but below decomposition temperatures of the blocks for a time sufficient to allow approach to the equilibrium morphology.

In solvent vapor annealing the sample is held in a controlled atmosphere containing selected solvent vapors. Absorption of the vapor imparts greater mobility within the film.

Directed self-assembly (DSA) methods

Conventional Lithographic Techniques



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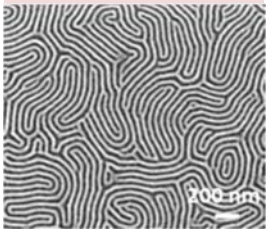
Block Copolymers



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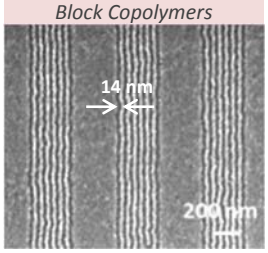
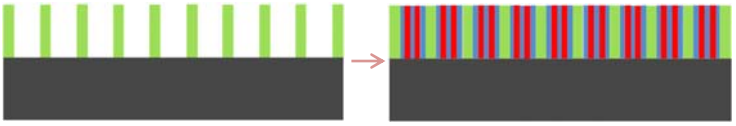
Directed Self-Assembly of Block Copolymers

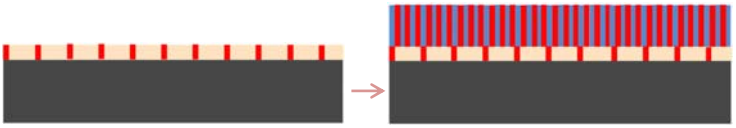


Methodologies to DSA

Graphoepitaxy



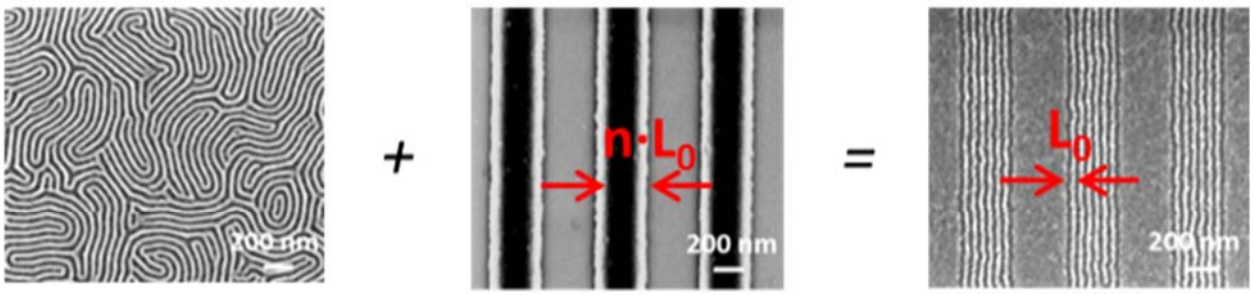
Chemoepitaxy



The **density multiplication** and **pattern rectification** are the main advantages of DSA, since they allow achieving dense patterns with tight size and placement tolerances, low defect densities and reduced e-beam writing times.

Directed self-assembly (DSA) methods

Density multiplication factor (n)



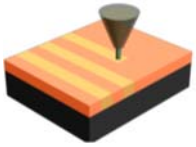
Intrinsic property of BCP to self-assemble

Graphoepitaxy process

Graphoepitaxy consists in creating **topographical features** on the substrate to enforce the self-assembly of block copolymers, thus enhancing the lateral order on the BCP nano-domains.

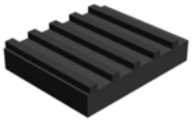
Graphoepitaxy overall process

1. E-beam lithography



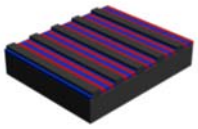
2. PMMA development + Si etching

3. Resist stripping



4. Brush deposition

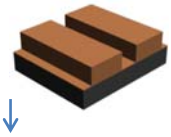
5. BCP spin-coating



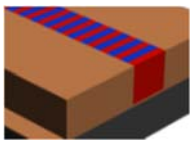
BCP morphology control inside the guiding patterns

The chemical affinities between the **walls** and the **bottom** with the **BCP nanodomains** are the ones which determine the orientation the BCP will take after self-assembly.

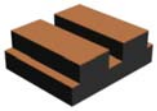
Neutral bottom and **neutral** walls



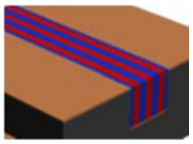
Perpendicular morphology **perpendicularly** oriented to trenches



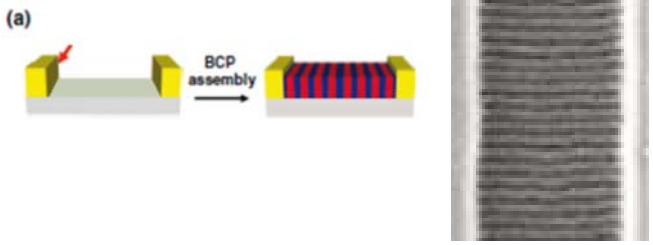
Neutral bottom and **preferential** walls

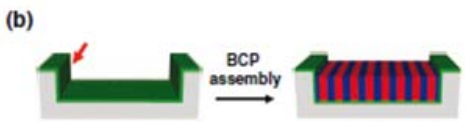


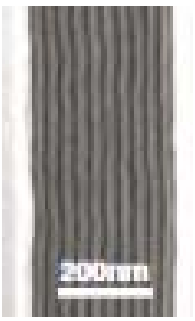
Perpendicular morphology **parallely** oriented to trenches



Examples of grapho-epitaxy







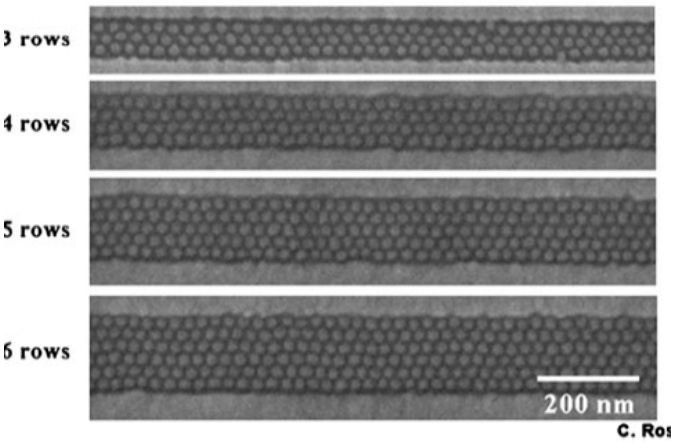


FIG. 4. Lithographically templated assembly of a polystyrene–polyferrocenyldimethylsilane (PS–PFS) diblock copolymer into a regular array of close packed structures, exhibiting short- and long-range order. Photographs courtesy of the research group of Ross and Chuang, Massachusetts Institute of Technology, adapted from Cheng, Nature Materials, 3(11), 824 (2004), used with permission.

Directed block copolymer self-assembly for nanoelectronics fabrication.
Daniel J.C. Herr.
J. Mater. Res., 26, 122, , 2011

Nano-confinement of block copolymers

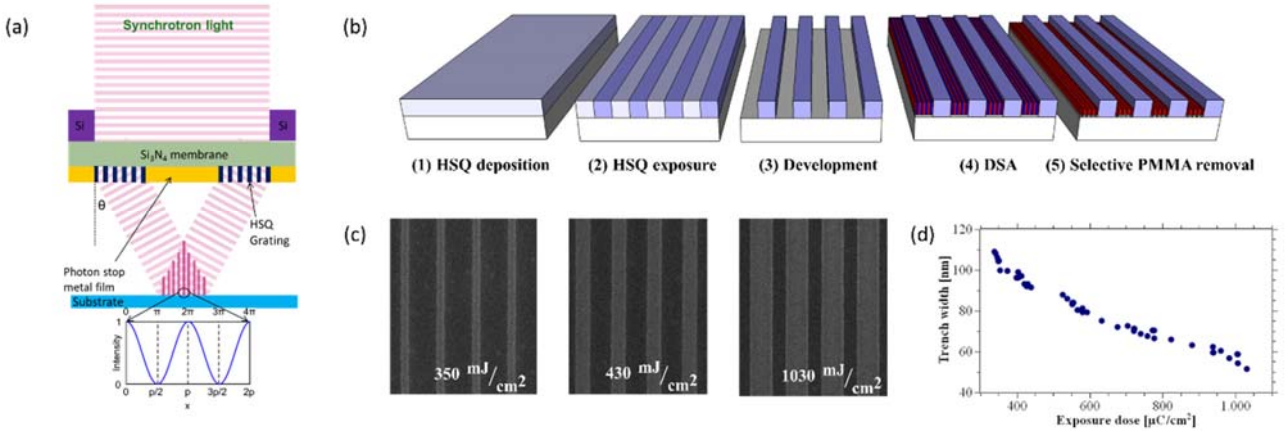
Soft Matter

PAPER

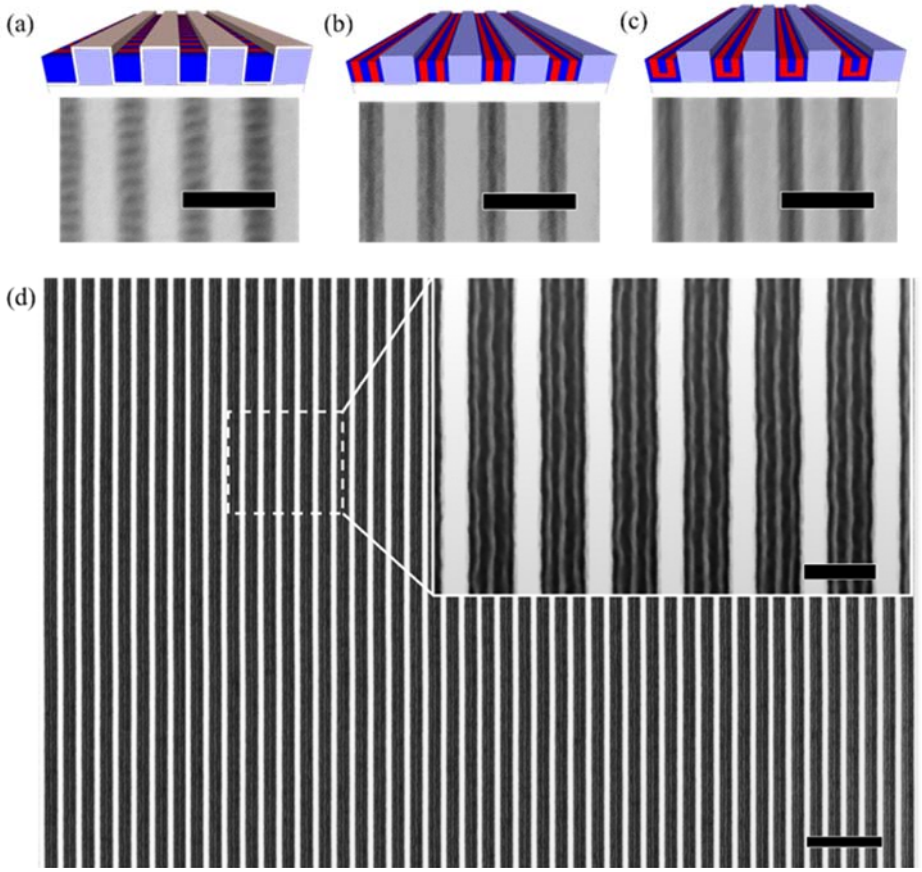
Cite this: DOI: 10.1039/c8sm01045e

Nano-confinement of block copolymers in high accuracy topographical guiding patterns: modelling the emergence of defectivity due to incommensurability†

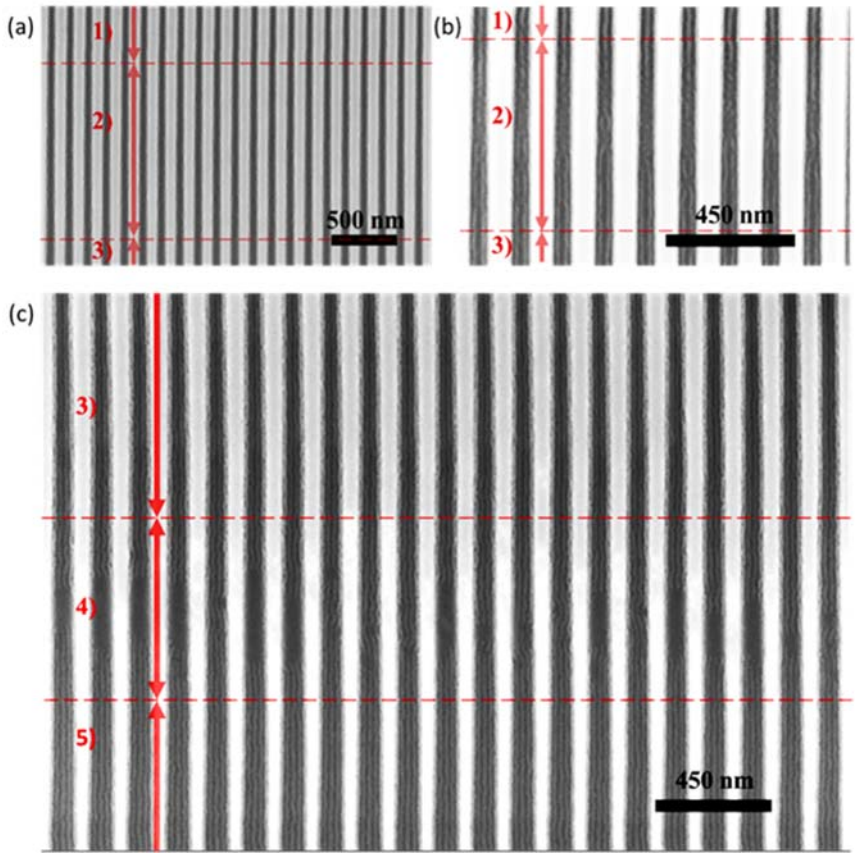
Steven Gottlieb,[a] Dimitrios Kazazis,[b] Iacopo Mochi,[b] Laura Evangelio,[a] Marta Fernández-Regúlez,[a] Yasin Ekinci[b] and Francesc Perez-Murano[a]

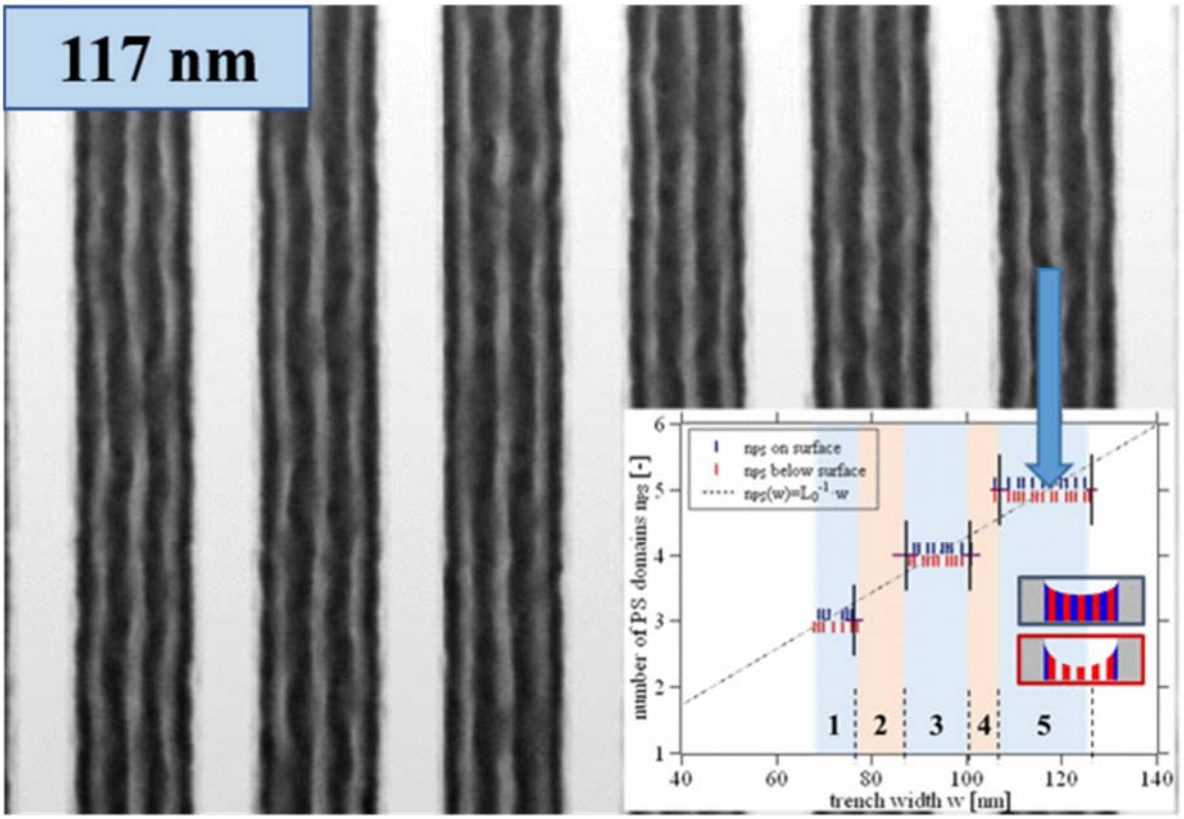


Nano-confinement of block copolymers

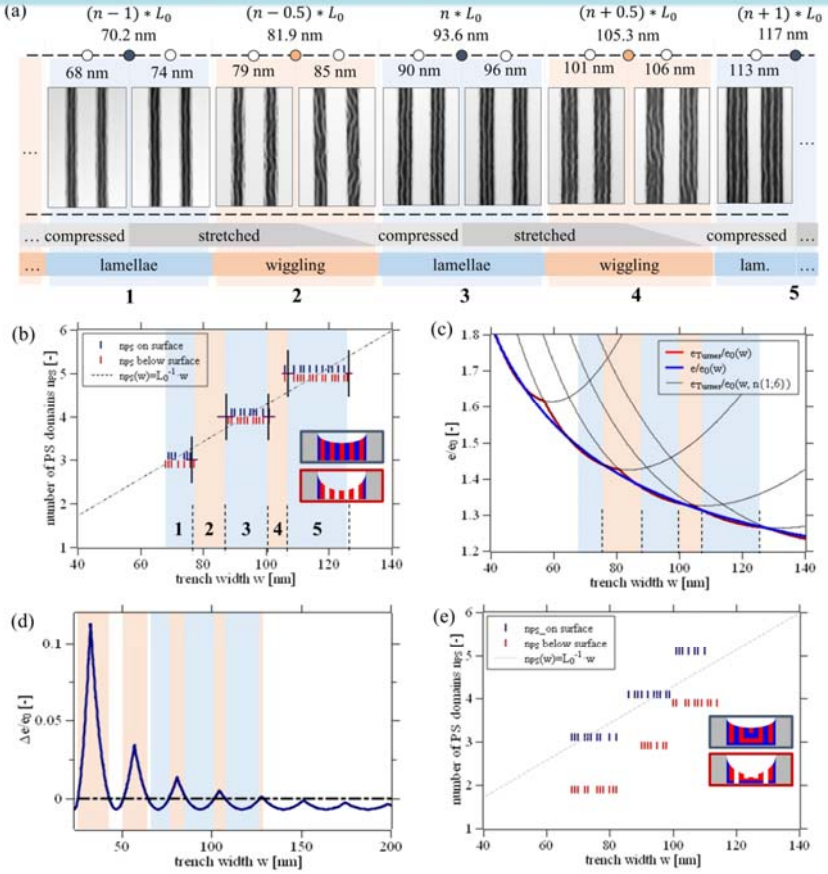


Examples of grapho-epitaxy



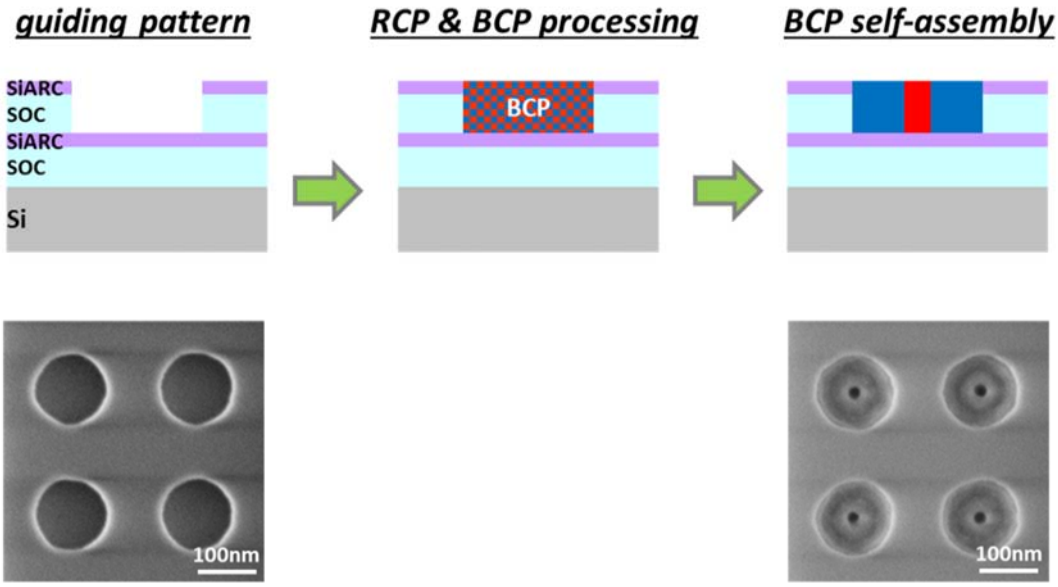


Nano-confinement of block copolymers



Graphoepitaxy process, contact shrink

Graphoepitaxy is commonly used for contact shrink applications, providing both the DSA capability to push further the optical resolution limit as well as to improve the lithography quality.



Tiron, R. et al. , "The potential of BCP's DSA for contact hole shrink and contact multiplication", Proc. SPIE, 8680, p. 868012 (2013)

Graphoepitaxy process, contact shrink

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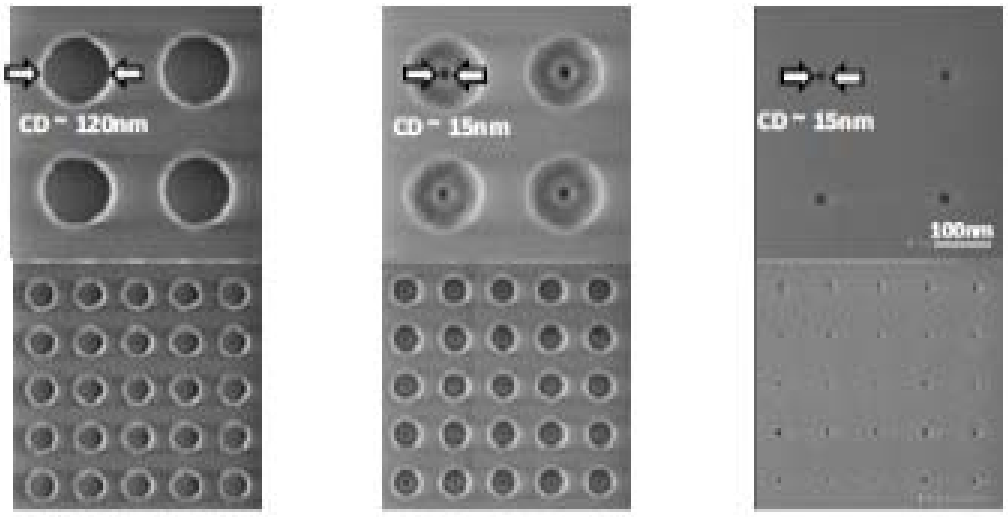


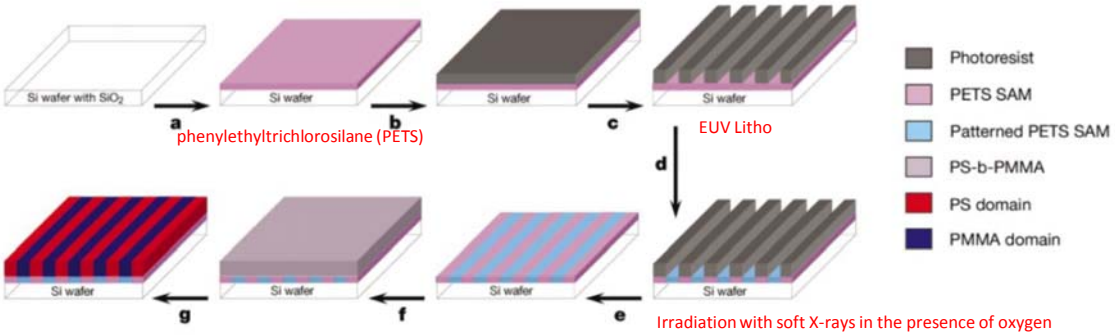
Tiron, R. et al. , "The potential of BCP's DSA for contact hole shrink and contact multiplication", Proc. SPIE, 8680, p. 868012 (2013)

Chemical epitaxy process (i)

Chemical epitaxy consists of a combination of a **top-down approach** to **create chemical patterns** with a self-assembled period process. It allows getting higher resolutions than the lithographic ones.

First chemoepitaxy approach based on SAM functionalization

Kim, S.O. de Pablo, Nealey. , "Epitaxial self-assembly of block copolymers on lithographically defined nanopatterned substrates", Nature, 424, 411-414 (2003)



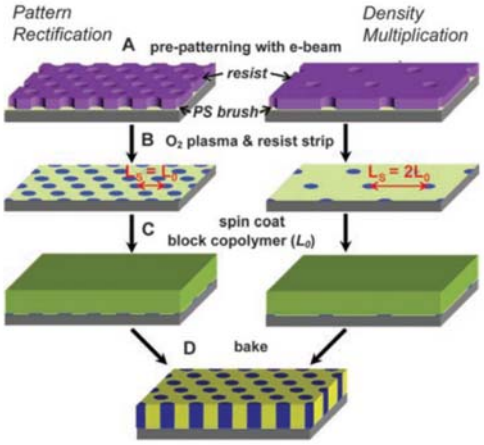
PS-b-PMMA copolymer
(Lo = 48 nm,film thickness of 60 nm)

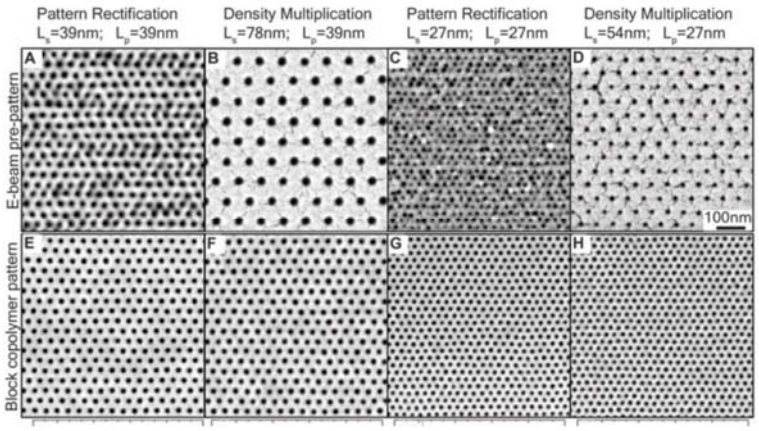
Chemical epitaxy process (ii)

Chemical epitaxy consists of a combination of a **top-down approach** to **create chemical patterns** with a self-assembled period process. It allows getting higher resolutions than the lithographic ones.

Creation of chemical guiding patterns by means of EBL and oxygen plasma functionalization

Ruiz, R. et al. , "Density multiplication and improved copolymer assembly", Science, 321, 936-940 (2008)



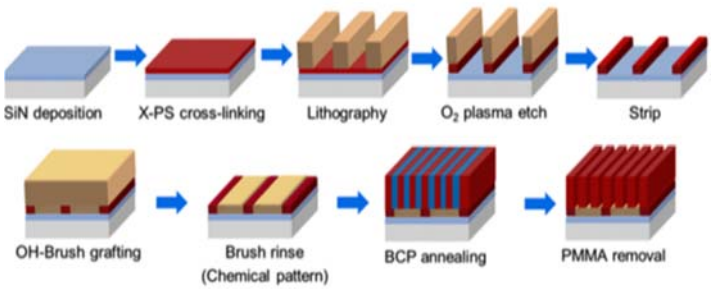


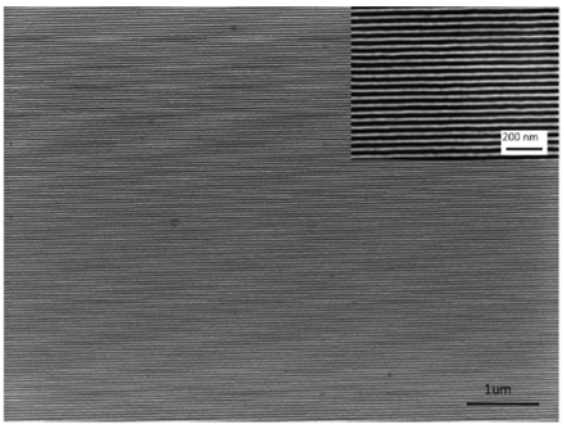
Chemical epitaxy process (iii)

Chemical epitaxy consists of a combination of a **top-down approach** to **create chemical patterns** with a self-assembled period process. It allows getting higher resolutions than the lithographic ones.

*Creation of chemical guiding patterns by using **two brush materials** (LiNe process)*

Liu, C-C. et al. , "Fabrication of Lithographically Defined Chemically patterned polymer brushes and Mats", Macromolecules, 44, 1876-1885 (2011)





PS-b-PMMA film directed to assemble on a chemical pattern comprised of X-PS guiding stripes and P(S-r-MMA) background with $f_s = 0.43$ and with $L_s = 2L_0$ and $W \sim 0.6L_0$

Chemical epitaxy process (iv)

Chemical epitaxy consists of a combination of a **top-down approach** to **create chemical patterns** with a self-assembled period process. It allows getting higher resolutions than the lithographic ones.

Creation of pinning sites in a neutral layer(AZ Smart process)

Kim, Jihoon et al., "The Smart TM process for Directed Block Co-Polymer Self-Assembly". Journal of Photopolymer Science and Tecnology, 26, 573-579 (2013)

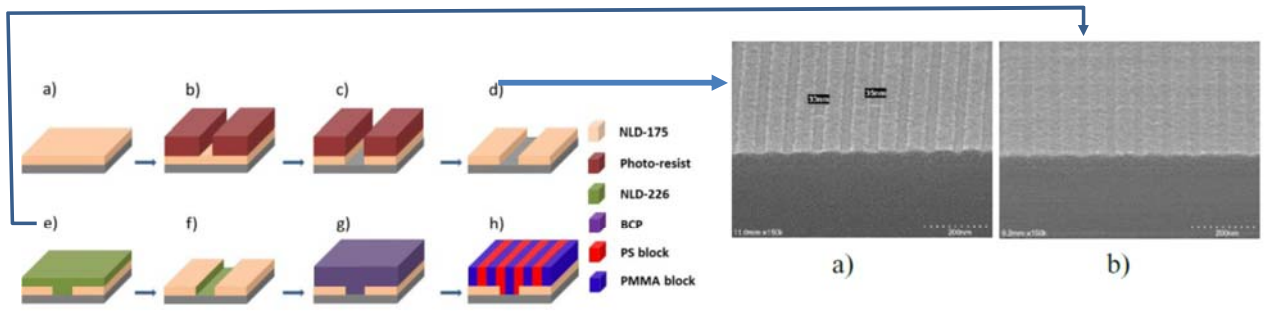


Fig. 7. xSEM of AZ SMART chemical pre-pattern structure a) before pinning material brushing and b) after pinning material brushing.

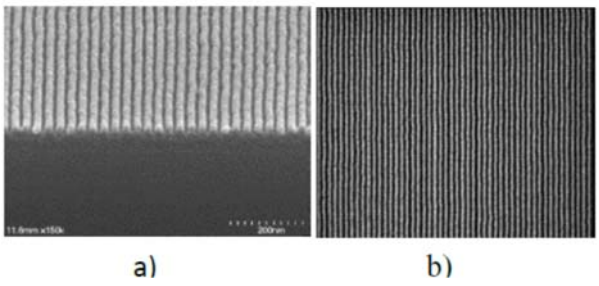
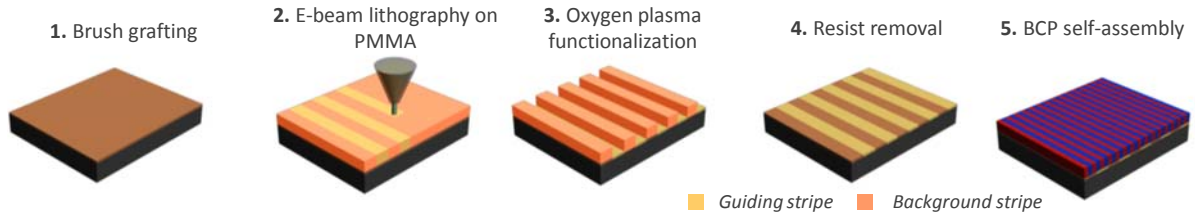


Fig. 8. DSA performance of AZ SMART flow with chemical pre-pattern repeating pitch of 90nm and trench width of 45nm (3x pitch multiplication, BCP Lo 30nm. a) x-section and b) top-down SEM images

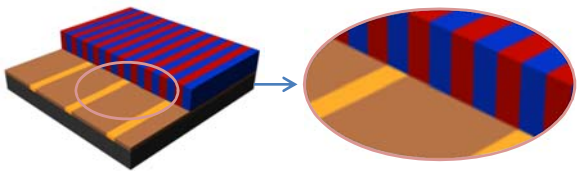
Chemical epitaxy process (v)

Chemical epitaxy overall process

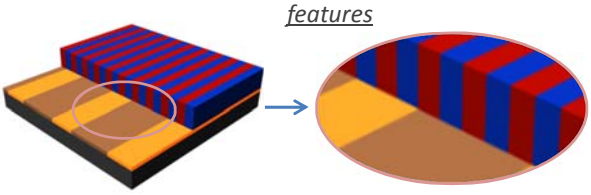


Density multiplication by using narrow and wide guiding stripes

*DSA using **narrow** guiding features*

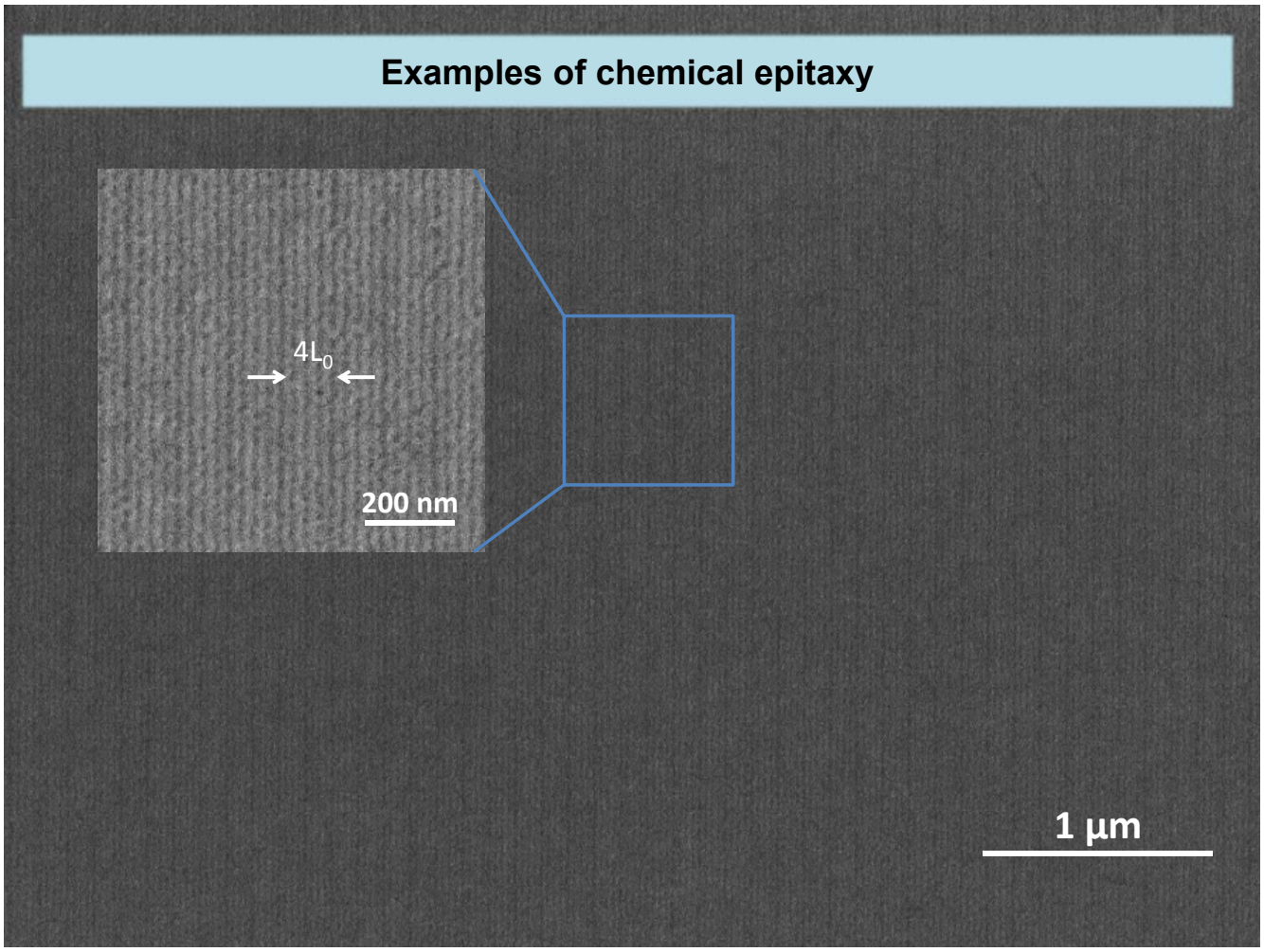


*DSA using **wide** guiding features*

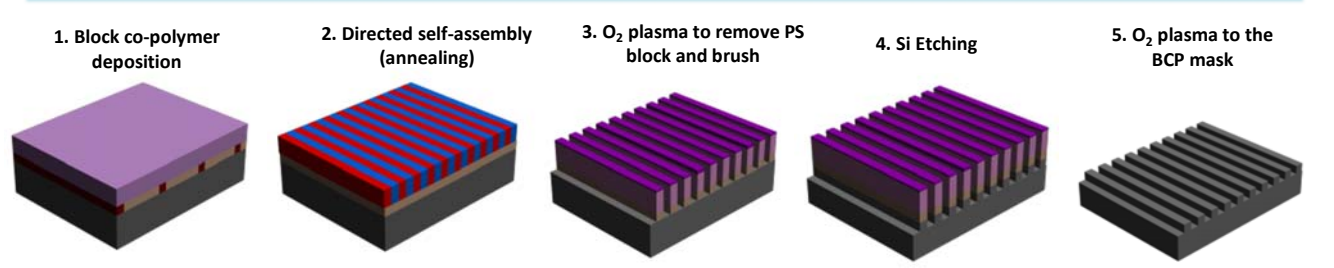


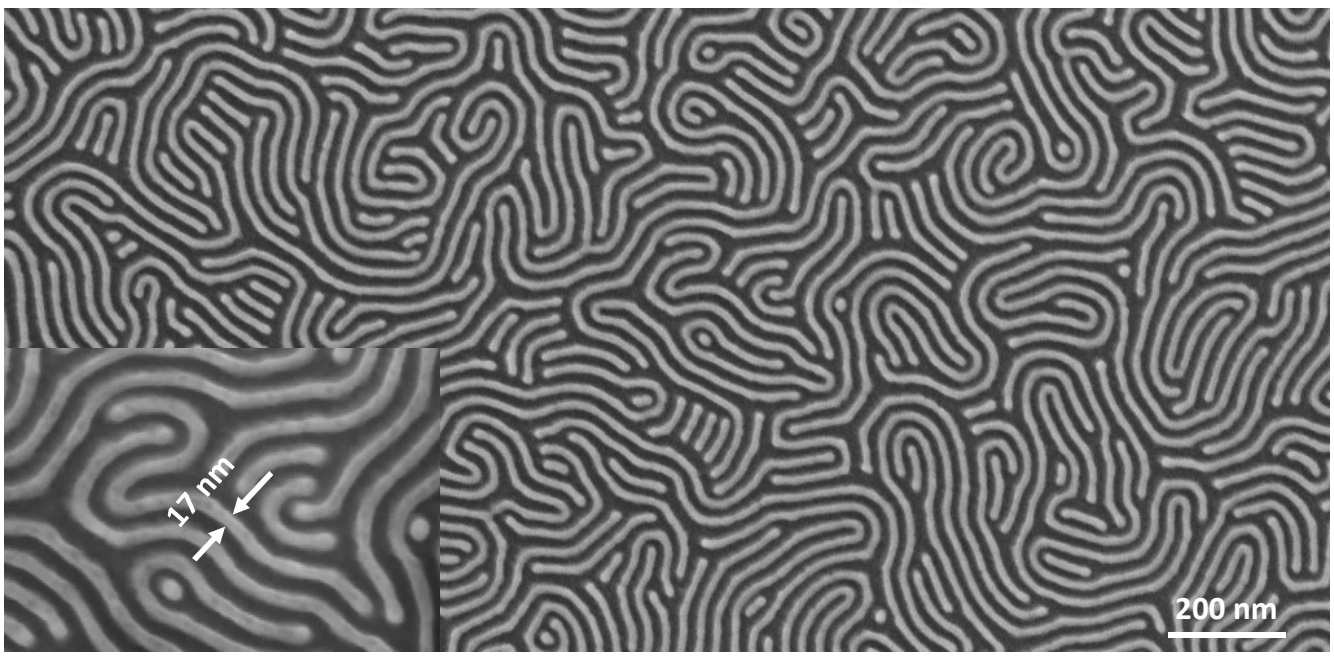
Schemes adapted from SIA Lithography Roadmap 2013 "*DSA techniques for Lines and Spaces*"

Examples of chemical epitaxy



Pattern transfer





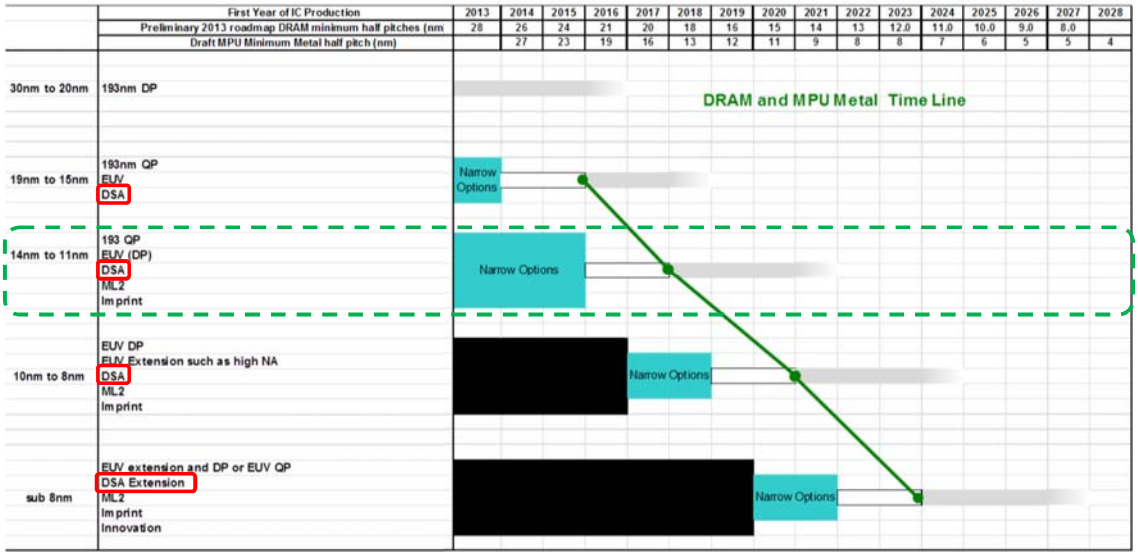
Applications

DSA IN THE 2013 ITRS ROADMAP LITHOGRAPHY

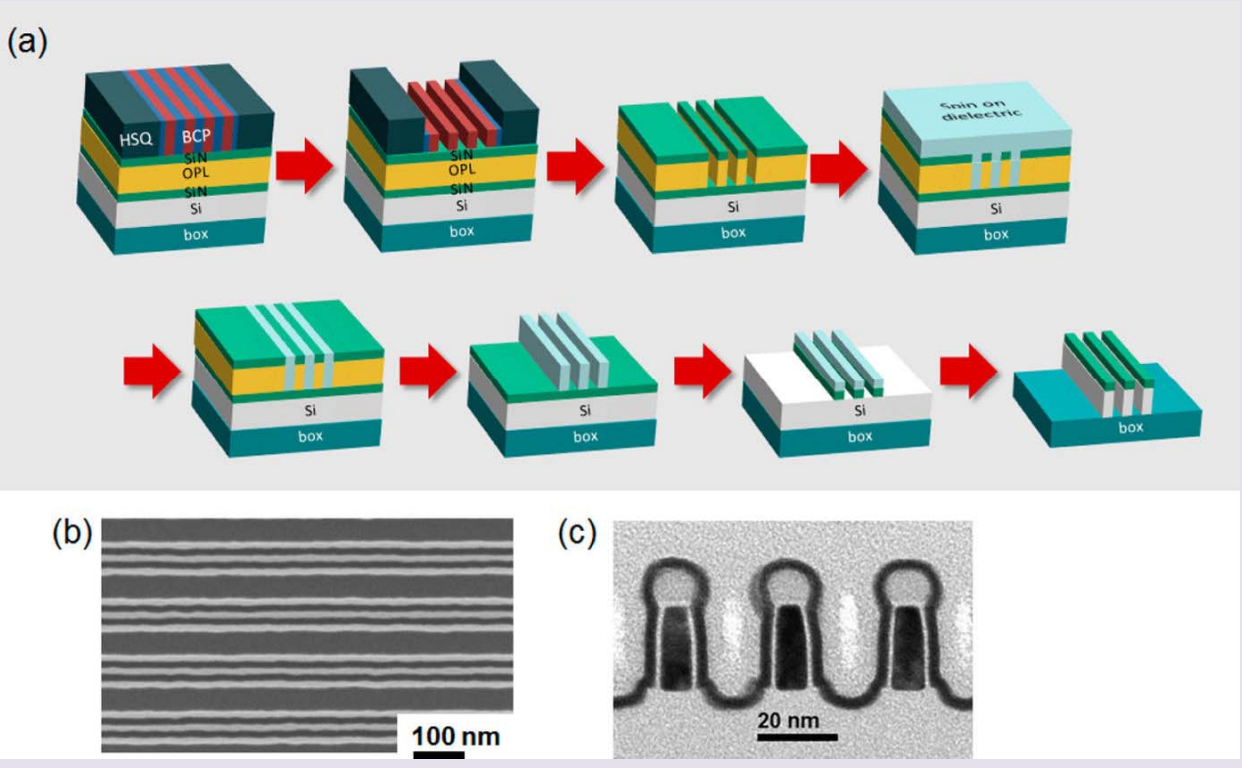
Development of methods for the controlled fabrication of nanoelectronic devices with:

- Critical dimensions below 10 nm (single digit fabrication)
- Potential to fulfill the future requirements of nanoelectronics industry

DSA of BCP in the 2013 ITRS Roadmap Lithography



Two-Dimensional Pattern Formation Using Graphoepitaxy of PS-b-PMMA Block Copolymers for Advanced FinFET Device and Circuit Fabrication



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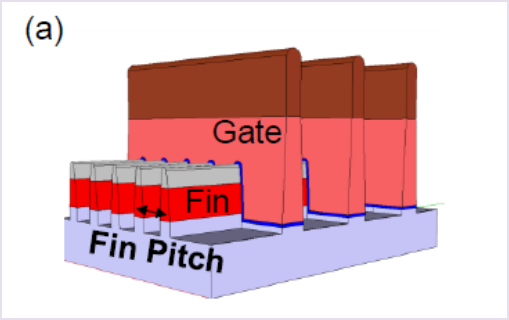
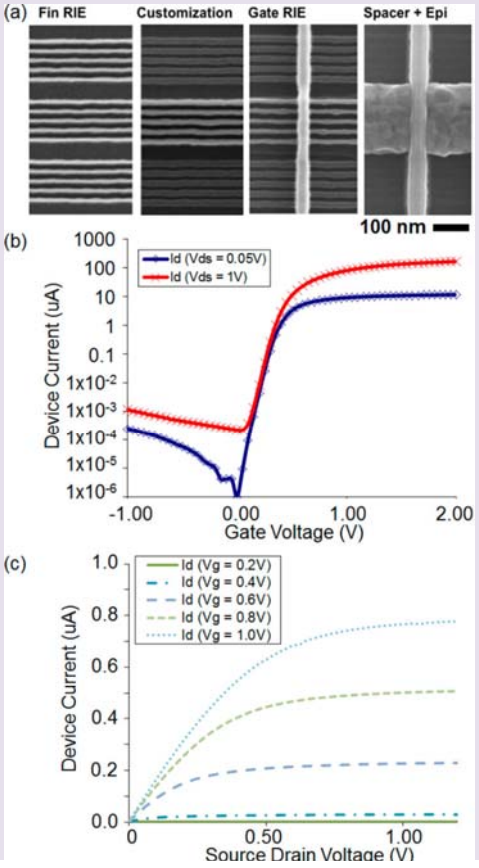
Two-Dimensional Pattern Formation Using Graphoepitaxy of PS-b-PMMA Block Copolymers for Advanced FinFET Device and Circuit Fabrication





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Applications

Bit patterned media

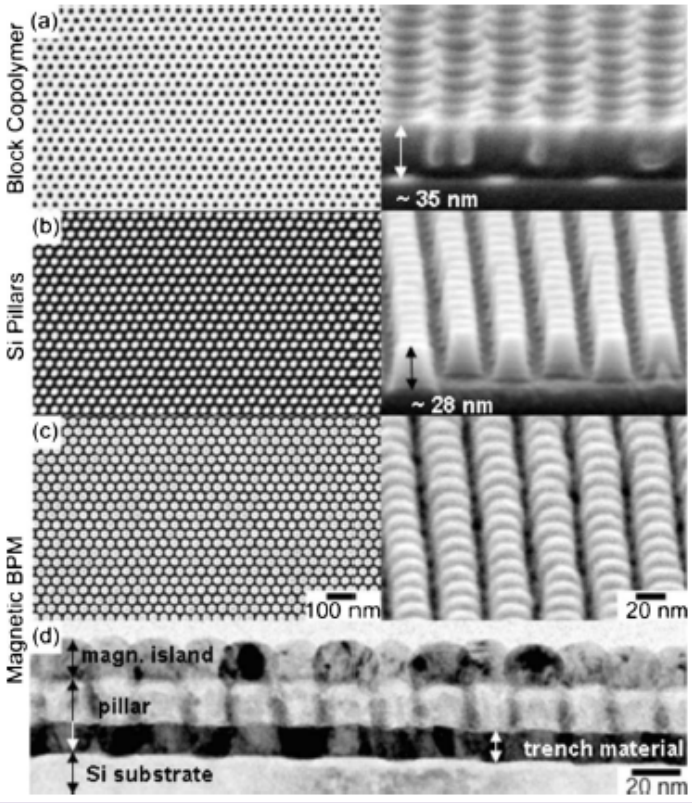

FIG. 1. 0.5 Tbit/in^2 (L_o=38 nm) BPM array consisting of MLs deposited onto Si pillar substrates fabricated via e-beam directed assembly of block copolymer films. SEM micrographs of (a) the block copolymer film after selective removal of the PMMA cylinder cores, (b) Si pillars after Cr lift-off using the template in (a) and subsequent reactive ion etching, and (c) magnetic BPM after depositing a Co/Pd ML thin film onto the pillar structures (left: top view, right: section view at 85° angle). (d) Bright field TEM cross-sectional image through two consecutive rows of bits (into the image plane) that are 180° phase shifted with respect to each other.

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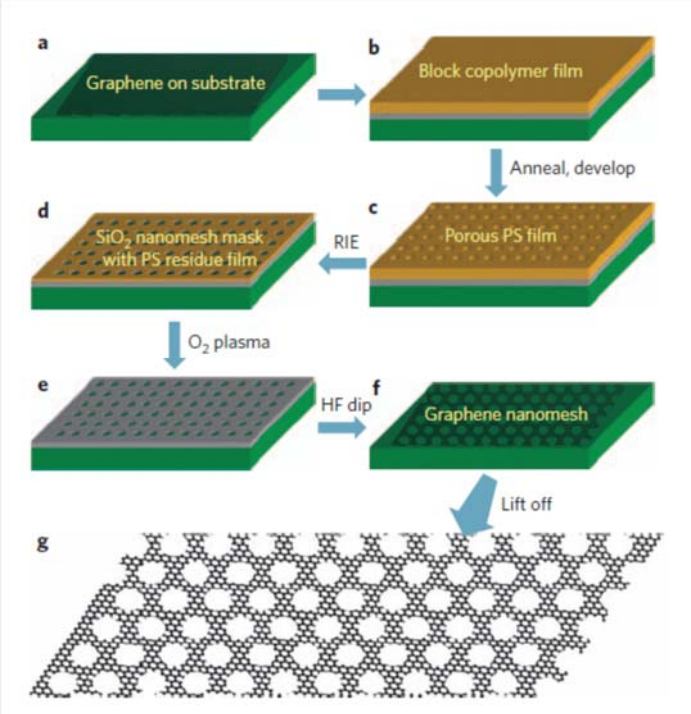
GRAPHENE NANOMESH

Graphene has significant potential for application in electronics, but cannot be used for effective field-effect transistors operating at room temperature because it is a semi-metal with a zero bandgap. Processing graphene sheets into nanoribbons with widths of less than 10 nm can open up a bandgap that is large enough for room-temperature transistor operation, but nanoribbon devices often have low driving currents or transconductances



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GRAPHENE NANOMESH

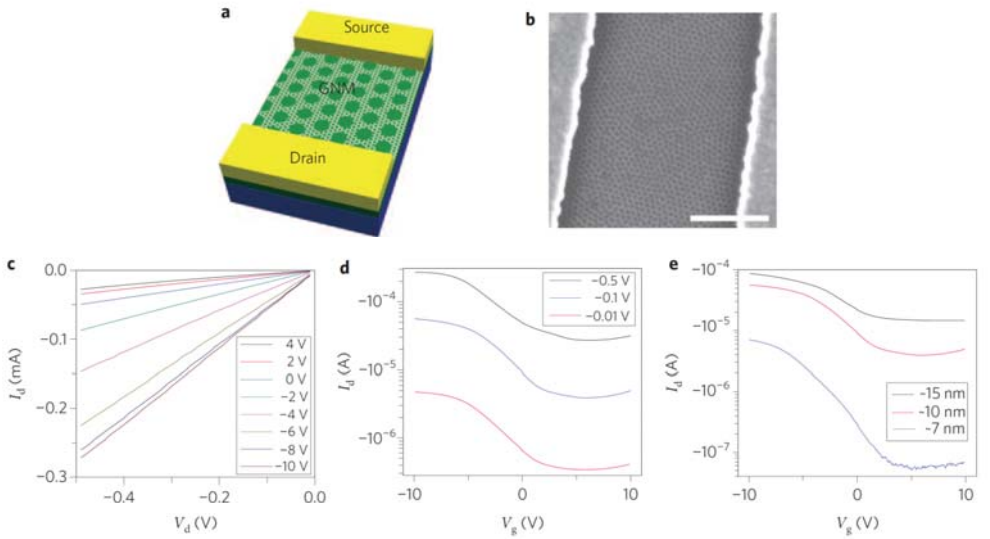

Figure 4 | Room-temperature electrical properties of a graphene nanomesh device. a, Schematic of a GNM-FET. The device is fabricated on a heavily doped silicon substrate with 300-nm SiO_2 as the gate dielectric. The electronic measurement was carried out in ambient conditions at room temperature, without removing the top oxide layer. **b**, SEM image of a GNM device made from nanomesh with a periodicity ~39 nm and neck width of ~10 nm. Scale bar, 500 nm. **c**, Drain current (I_d) versus drain–source voltage (V_d), recorded at different gate voltages for a GNM device with a channel width of ~2 μm and channel length of ~1 μm. The on-state conductance at $V_g = -10$ V is comparable to an array of 100 parallel GNR devices. **d**, Transfer characteristics for the device in **c** at $V_d = -10$ mV, −100 mV and −500 mV. The ratio between I_{on} and I_{off} for this device is ~14 at $V_d = -100$ mV. **e**, Transfer characteristics at $V_d = -100$ mV for GNMs with different estimated neck widths of ~15 nm (device channel width 6.5 μm and length 3.6 μm), ~10 nm (channel width 2 μm and length 1 μm) and ~7 nm (channel width 3 μm and length 2.3 μm).

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Summary on DSA

- Simple method to create nanopatterns on surfaces
- Resolution is dictated by the size of the molecules
- Interface energies plays a key role to obtain a proper alignment
- Defectivity limits applicability on high volume manufacturing
- Other applications are being developed

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MICRO nano FABS